Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 238-239

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Improving the Cell Characteristics Using SiN Liner at Active Edge in 4 G NAND Flash

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Introduction

Recently the cell integration density of NAND flash memory is increasing rapidly due to its simple structure suitable for high resolution lithography. Therefore, the reduction of cell size has been the most important issue. However, with the increase in the number of the cells and the scaledown of the cell size, the NAND cell string has some problems such as small on-cell current and poor cell V_{th} distributions [1],[2]. Also, it was well known that they are related to corner of active edge [2-4]. In this work, we have improved not only the on cell current but also cell V_{th} distributions by using SiN liner to side wall of field oxide.

Experimental

The conventional SAP (Self Aligned Floating Poly) process flow to form oxide liner to active edge is shown in Fig. 1 [5]. After pad oxidation, SiN and hard mask is formed and active/field is patterned by lithography and dry etch. After that oxide liner is deposited through LP-CVD as shown in Fig. 1(a). As shown in Fig. 1(b), STI (Shallow Trench Isolation) is formed by HDP (High Density Plasma) and oxide-CMP (Chemical Mechanical Polishing). SiN and pad oxide are removed by wet etch as shown in Fig. 1(c). After tunnel oxide is grown through radical oxidation and poly-silicon is deposited, floating gate is formed through poly- silicon CMP process. After field oxide between floating gates was removed by wet etch, ONO and control-gate is deposited as shown in Fig. 1(d). The new process flow to form SiN liner to active edge is shown in Fig. 2. After trench is formed, oxide and SiN liner(50Å) liner is deposited through LP-CVD as shown in Fig. 2(a). In order to conduct oxide-CMP, SiN on active mask is removed by dry etch. As shown in Fig. 2(b), STI is formed by HDP and oxide-CMP. After SiN and pad oxide are removed by wet etch as shown in Fig. 2(c), tunnel oxide and floating gate is formed. The field oxide between floating gates was removed by wet etch down to a level above the top of SiN liner. After that, ONO and control gate is deposited as shown in Fig. 2(d). The profile of active edge was observed by SEM (Scanning Electron Microscope) and TEM (Transmission Electron Microscope). The endurance characteristics of NAND flash cell were measured in TEG (Test of Elements Group) pattern and characteristics of bake retention was conducted in 64 M cell pattern.

Results

Fig. 3 and Fig. 4 show the best/worst on cell current at read voltage of 4.0, 4.5, 5.0, 5.5 V with oxide and SiN liner. The on cell current of the SiN liner is larger than that of oxide liner due to increased capacitance of tunnel oxide. Fig. 5 shows the simulation results with ATHENA simulator about process in Fig. 1 and 2 [6]. C_{tun}.(SiN liner)=703 aF and C_{tun}(oxide liner)=683 aF was obtained from ATLAS simulator for the device in Fig. 5 (a), (b) respectively [6]. Also, the electric field at active edge was obtained for erasing and programming state as shown in Fig. 6 and Fig. 7 [6]. The electric field at active edge is decreased by SiN liner [7]. Fig. 8 shows the active edge profile of tunnel oxide. Oxide thickness of SiN liner process is 4Å thicker than that of conventional process by SiN liner stress [8]. Fig. 9 compares the cell V_{th} distribution of 64 M bits cell by ISPP (Incremental Step Pulse Program). The cell V_{th} distribution was improved with SiN liner due to the decreased electric field and increased thickness of tunnel oxide at active edge [2]. Fig. 10 shows the I_d-V_g curves of GSL (Ground Select Line) transistor, which controls the CSL (Common Source Line) [1]. The subthreshold slope of SiN liner is improved due to increased tunnel oxide capacitance. Also, I_{off} of transistor with SiN is decreased. Fig 11 shows the simulation result of boron concentration with oxide and SiN liner. The higher boron concentration around active edge with SiN liner causes the lower I_{off}. The endurance characteristics of SiN liner in comparison to oxide liner are shown in Fig. 12. After 10^5 program/erase cycling at TEG cell, negligible differences in the threshold voltage shift between the SiN liner and oxide liner was observed. Also, as shown in Fig. 13, bake retention results which are obtained after 10^4 program/erase cycles followed by baking at 250 °C for 2 hours are improved.

Summary

For the first time, we proposed the SAP process using the SiN liner at active edge to improve the cell characteristics of high density NAND flash memory devices. As shown in Table 1, the cell current is increased by increased capacitance of tunnel oxide. Also, we could confirm the cell V_{th} distributions are improved due to the decreased electric field and increased tunnel oxide thickness at active edge. The fabricated cell also showed significant improvement in bake retention.

References

[1] J. Lee et al., IEEE J. Solid-State Circuits, Vol. 38, pp 1934-1942, Nov. 2003.
[2] D.W. Kang et al., NVSMW, pp. 40-41, 2004.
[3] H. Watanabe et al., IEDM Tech. Dig., pp 833-836, 1996.
[4] T. Park et al., Symp.on VLSI Tech., pp 159-160, 1999.
[5] J.H. Park et al., IEDM Tech. Dig., pp 873-876, 2004.
[6] ATHENA process and ATLAS Device simulator in SILVACO.
[7] Takaaki Aoki et al., Proc. of 18th ISPSD & IC's, June 2006.
[8] K.S. Lee et al., IRPS, pp 121-125, 2003.

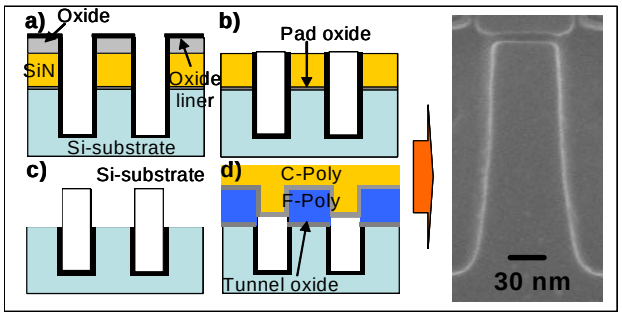

Fig. 1 The conventional process flow of oxide liner.

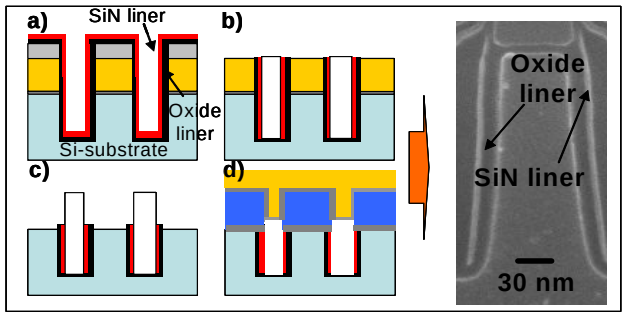

Fig. 2 The new process flow of SiN liner.

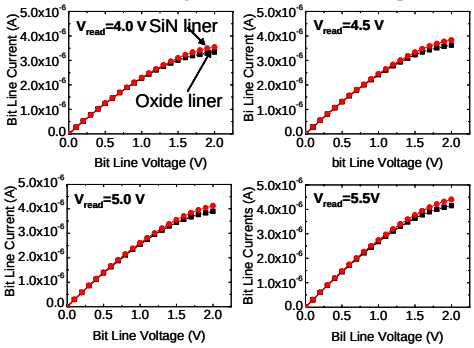

Fig. 3 The best on cell current characteristics(other cells are erased).

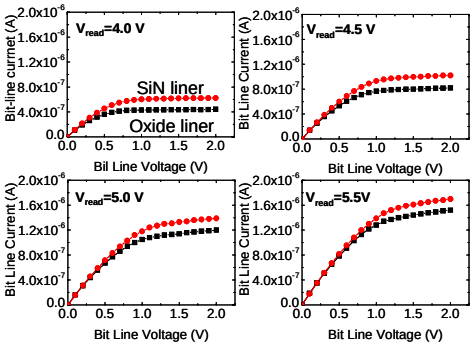

Fig. 4 The worst on cell current characteristics(other cells are programmed).

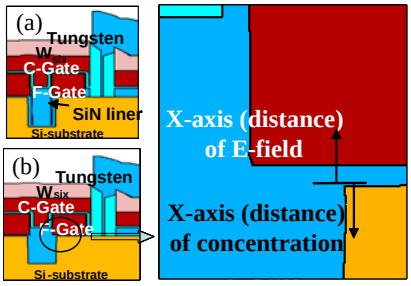

Fig. 5 The results of Athena simulation about Fig. 1, 2 process. (a) SiN liner, (b) oxide liner.

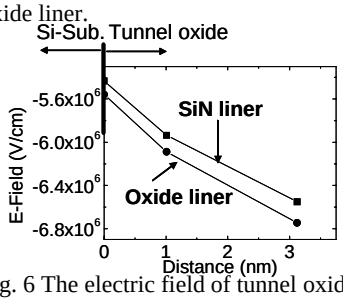

Fig. 6 The electric field of tunnel oxide at active edge for erase state.

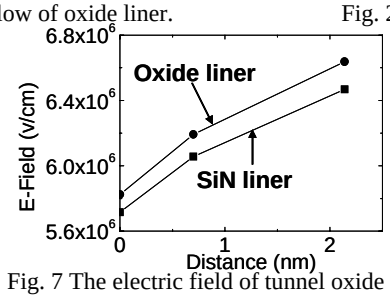

Fig. 7 The electric field of tunnel oxide at active edge for program state.

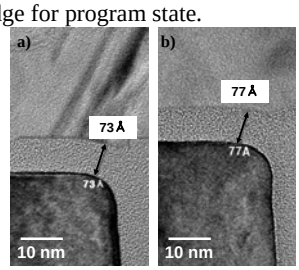

Fig. 8 TEM image of active edge. (a) Oxide liner. (b) SiN liner.

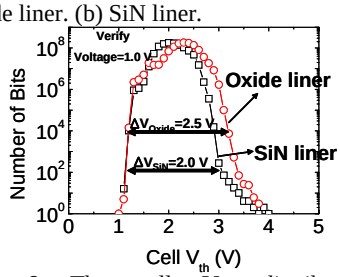

Fig. 9 The cell V_{th} distribution characteristics.

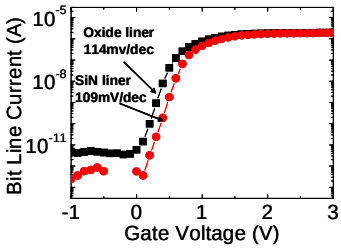

Fig. 10 I_d-V_g curves and sub-threshold slope of GSL.

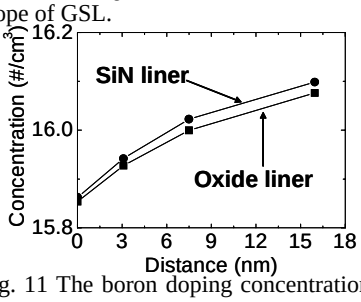

Fig. 11 The boron doping concentration at active edge.

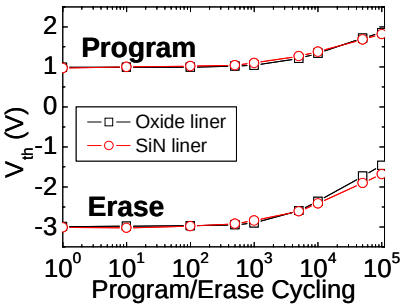

Fig. 12 The endurance characteristics after 10^5 P/E cycling.

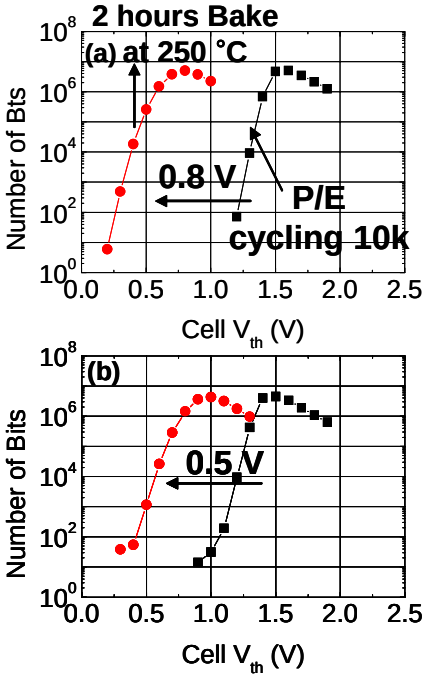

Fig. 13 The bake retention characteristics after 10 K P/E cycling and 250 °C for 2 hours. (a) Oxide liner (b) SiN liner.

Table 1 The summary of electrical characteristics.

Type	State	SiN liner	Oxide liner
Cell Current (uA)	Worst Situation (V_{read}=5.5 V, $V_{bit\ line}$=1.0 V)	1.71 uA	1.52 uA
	Best Situation (V_{read}=5.5 V, $V_{bit\ line}$=1.0 V)	4.41 uA	4.15 uA
I_{off} of GSL Transistor (A)	-	5.9×10^{-13} A	5.5×10^{-12} A
Cell V_{th} Distribution (V)	ΔV_{th}	2.0 V	2.5 V
Bake Retention at 250 °C for 2 hours	ΔV_{th} shift (10^4 cycling)	0.5 V	0.8 V