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Nanocrystal floating gate memory devices using atomic layer deposited TiN/Al_2O_3 nanolaminate layers

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1. Introduction

Nonvolatile memory (NVM) devices with a low operation voltage, consuming less power and allowing higher integration with high-speed writing and erasing of data are highly demanded in the semiconductor industry for future nano-scale flash memory device applications [1]. Due to high charge loss and scaling problem in polycrystalline silicon-oxide-silicon-nitride (Si_3N_4)-oxide-silicon (SONOS) flash memory devices [2], high-κ charge trapping layers such as HfO_2, HfAlO, nanolaminate layers in metal-[aluminum-oxide]-high-κ- oxide-silicon (MAHOS) structure have been reported [3-5]. To improve the charge loss, many metal nanocrystals [6-8] are also reported recently. High density and highly uniform metal nanocrystals with a small size (diameter <5 nm) are demanded in the semiconductor market for future nano-scale NVM device applications. It is strongly believed that the floating gate memory devices with nanocrystals can be scaled beyond 32 nm technology node. In this study, high-density and highly uniform atomic layer deposited (ALD) TiN metal nanocrystals embedded in high-κ Al_2O_3 layers are reported for possible future low power and multi-level charge storage flash memory device applications

2. Experimental

The starting wafer was p-type Si (100) with a resistivity of 15-25 Ω.cm. Prior to deposition of tunneling oxide (SiO_2), the p-Si wafers were cleaned by the RCA process. The tunneling oxide with a thickness of 3 nm was grown by the RTO system at 1000°C for 20s. Then, TiN (0.5 nm)/Al_2O_3 (1 nm) nanolaminate layers with 7 periods were deposited by plasma-enhanced atomic layer deposition (PEALD)/atomic layer deposition (ALD) cluster tools. Then, the high-κ Al_2O_3 blocking oxide with a thickness of 20 nm was deposited by ALD. Schematic memory structure of TiN/Al_2O_3 nanolaminate layers is shown in Fig. 1. The post deposition annealing was performed at 900°C for 2 min in N_2 (90%) and O_2 (10%) gases. For comparison, a pure HfO_2 charge trapping layer with a thickness of 10 nm was deposited on SiO_2 (3 nm)/p-Si substrate. Then, the Al_2O_3 blocking oxide with a thickness of 10 nm was on HfO_2 charge trapping layers. A pure Al_2O_3 charge trapping layer with a thickness of 20 nm was also deposited on SiO_2 (3 nm)/p-Si substrate for comparison. The pure HfO_2 and Al_2O_3 charge trapping layers were annealed at 900°C for 1 min in N_2 ambient. All high-κ films were deposited by ALD. A platinum (Pt) gate electrode with a area of $1.12x10^{-4}$ cm^2 was deposited by sputtering using shadow mask. The post metal annealing was performed at a substrate temperature of 400°C for 5 min in N_2 (90%) and H_2 (10%) gases.

3. Results and discussion

Fig. 2 shows a high-resolution transmission electron microscopy (HRTEM) image of TiN nanocrystal embedded in high-κ Al_2O_3 films after 900°C for 2 min process. A small size of TiN nanocrystals with a diameter of < 3 nm and a high-density of ~$5x10^{12}$/cm^2 have been observed due to TiN (0.5 nm)/Al_2O_3 (1 nm) nanolaminate layers. The TiN nanocrystals embedded in high-κ Al_2O_3 films have been confirmed by x-ray photoelectron spectroscopy measurement (not shown here). Fig. 3 shows the capacitance-voltage (C-V) hysteresis characteristics with different sweeping gate voltages. A large hysteresis memory window of $\Delta V \approx 15$ V is observed under an operation voltage of $V_g \approx \pm 10$ V, due to high-density of TiN nanocrystals. A significant memory window of $\Delta V \approx 0.9$ V with an extremely low gate voltage operation of $V_g \approx \pm 1$ V is also observed due to high work function ($\Phi_m \approx 4.68$ eV) of TiN nanocrystals (Fig. 4). It can provide the 0.6 eV deeper traps than that of Si nanocrystal, which has great impact to improve program/erase speed and retention characteristics. The capacitance density is high ~3.5 fF/μm^2. A flat-band voltage shift (ΔV_{FB}) of ~8 V for TiN nanocrystals is higher than that of pure HfO_2 and Al_2O_3 charge trapping layers (Fig. 5). The charge density of TiN nanocrystals is calculated using the equation: $Q_{charge}=C_{ox}$ x $(+V_{FB})$=~$2.8x10^{13}$/cm^2 (Fig. 6), where C_{ox} is the maximum capacitance at accumulation region. The charge density is higher than that of the nanocrystal density, and it may be due to unobserved molecular size nanocrystals by HRTEM image. The charge density and hysteresis memory window of TiN nanocrystals are very high as compared with pure HfO_2 and Al_2O_3 charge trapping layers (Fig. 7). The high uniformity of atomic layer deposited TiN nanocrystals is observed (Fig. 8), suggesting that it can be applied in future nano-scale flash memory device applications. The hysteresis memory windows on nanocrystal memory devices are not changing significantly at high measurement temperature, due to low leakage current in the memory structure. The leakage current of nanocrystal memory devices increases (slightly) with increasing the measurement temperature, due to Al_2O_3 blocking oxide and Pt metal gate (Fig. 9). To get a 3V programming/erasing state at 10 μs, a small operation voltage of V_g<5 V is necessary due to high work function and high-density TiN nanocrystals (Fig. 10). The discharge characteristics of all memory devices are shown in Fig. 11. The charge loss of nanocrystal devices is lower than that of pure HfO_2 and Al_2O_3 charge trapping layers, which has great impact in future NAND floating gate memory applications. A large memory window of ~4.6 V is observed after 10 years of retention (Fig. 12), due to nanoconfinement of charges in the metal nanocrystals. A low charge loss of 9% is observed after 10 years of retention. The large memory window with a low charge loss of nanocrystal memory devices have strong potential in future nano-scale multi-level charge (MLC) storage memory device applications.

4. Conclusions

The floating gate flash memory devices with a large memory window of 15 V, high program/erase speed of $\Delta V \approx 3$ V@ V_g<5V, 10 μs, low charge loss of 9%, and high-performance of atomic layer deposited TiN nanocrystal memory devices have been reported. A large memory window of 4.6 V is observed after 10 years of retention. Due to high uniformity, small size, and high-density of TiN nanocrystals, it can be used in future NAND and MLC flash memory device applications for mass production.

References

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[8] S. Maikap, et al., IEDMS, p. 85, 2006.

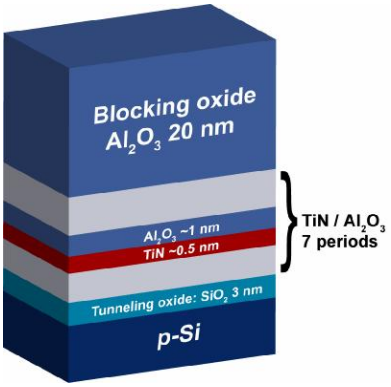

Fig. 1 Memory structure of ALD TiN (0.5 nm)/Al_2O_3 (1 nm) multilayers on SiO_2 (3 nm)/p-Si substarte. The thickness of Al_2O_3 blocking oxide was 20 nm.

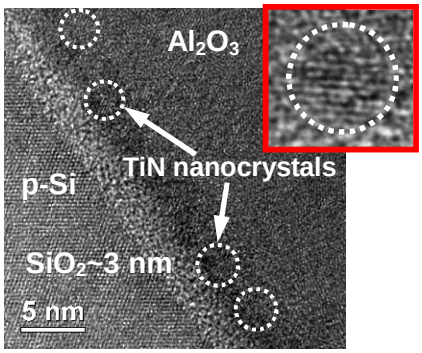

Fig. 2 Cross-sectional HRTEM image of atomic layer deposited TiN nanocrystals after 900°C, 2 min process. The diameter of TiN nanocrystal is less than 3 nm (in the inset).

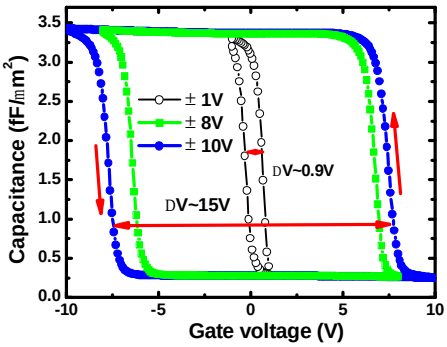

Fig. 3 The C-V (1 MHz) hysteresis shows a large memory window of ~15V@ V_g= ± 10 V. The hold time was 100 ms during C-V measurement.

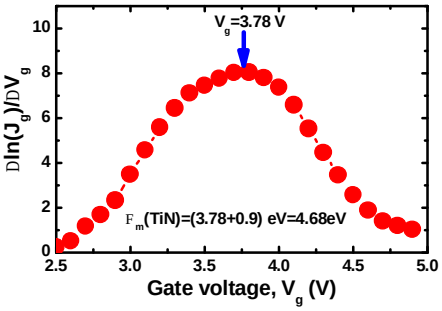

Fig.4 Current density (J_g) versus gate voltage (V_g) characteristics is measured using Si/Al_2O_3 (8 nm)/TiN structure. The calculation of work function (Φ_m) for TiN metal layers has been explained in the ref. [8].

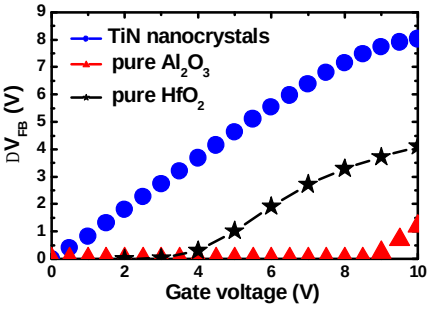

Fig. 5 V_{FB} shift as a function of positive gate voltage. The TiN nanocrystal shows large V_{FB} shift, while the pure Al_2O_3 does not show any hysteresis memory window up to gate voltage of 9 V.

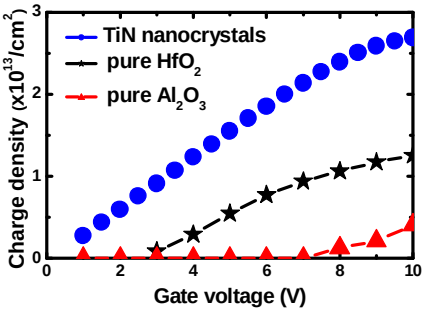

Fig. 6 Charge density as a function of positive gate voltage. The pure Al_2O_3 has negligible charge trapping density as compared with nanocrystal memory capacitors.

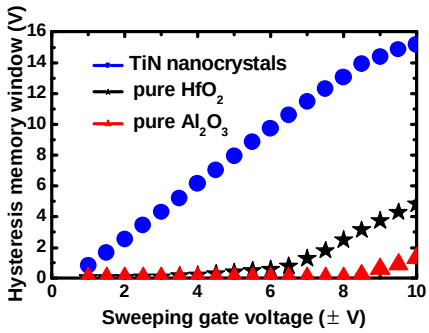

Fig. 7 Hysteresis memory window versus sweeping gate voltage for all memory devices.

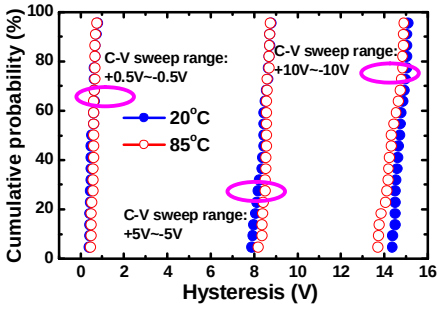

Fig.8 Cumulative probability of C-V hysteresis of TiN nanocrystal memory capacitors.

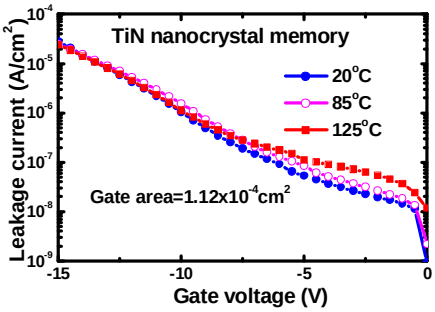

Fig. 9 A negligible leakage current increases with increasing measurement temperature, due to the Al_2O_3 blocking oxide and Pt gate.

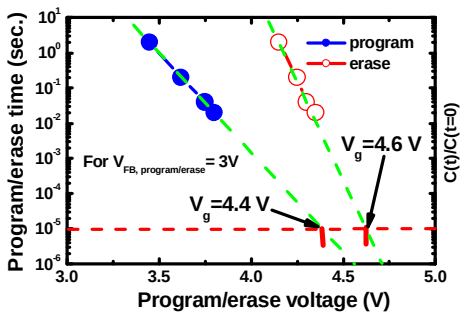

Fig. 10 Program/erase characteristics with high work function metal gate (Pt). The TiN nanocrystal memory device can be used for very low power applications.

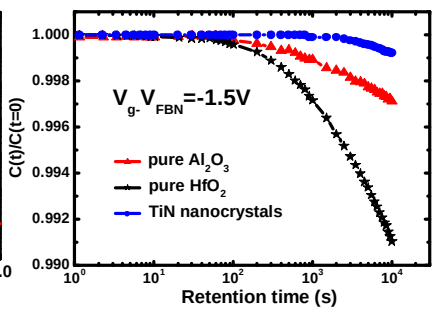

Fig. 11 Discharge characteristics of nanocrystal memory devices. Discharges are studied after V_g–V_{FBN} = 6V, 10s stressed condition. The V_{FBN} is the V_{FB} at neutral C-V (no hysteresis memory window).

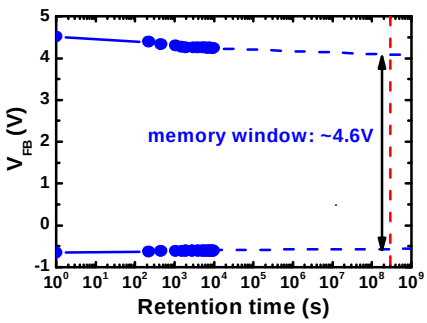

Fig. 12 Retention characteristic of nanocrystal memory devices. A large memory window is observed after 10 years of retention.