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Memory Window Enhancement of MOS Memory Devices with High Density Self-Assembled Tungsten Nano-dot

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1. Introduction

Many researches on non-volatile memory device with nanocrystal materials as charge storage node have been carried out recently. Among such memory devices, metal nano-dot memory has attracted much attention due to its superior retention characteristics caused by larger work-function of metal in comparison to those of Si or Ge nanocrystal. However, the density of metal nano-dot in previous papers [1] is not sufficiently high. Therefore, both magnitude and uniformity of memory window are not enough to achieve stable memory operation.

In this work, a self-assembled nano-dot deposition (SAND) method [2] has been employed for the formation of high-density tungsten nano-dots (W-ND) dispersed in SiO_2 matrix. Electrical characteristics of $Al/SiO_2/W\text{-}ND/SiO_2/p\text{-}Si$ MOS memory devices are investigated in detail. Furthermore, thermal effects for metal nano-dot characteristics are also studied.

2. Experimental

Our MOS memory device with tungsten nano-dot (W-ND) was fabricated through process flow as shown in Fig. 1. An 8-nm-thick W-ND layer was self-assembled using SAND method on a 4.6-nm-thick thermally oxidized silicon substrate. Fig. 2 shows the schematic of SAND method using special sputtering with metal chip and insulator target. Subsequently, a blocking silicon dioxide with 12-nm-thick was deposited by TEOS CVD at 720 ^oC. To study thermal effects, the post-deposition annealing (PDA) was performed at 900 ^oC for 30 minutes in N_2 ambient for some sample. Finally, Al electrode was evaporated, followed by post-metallization annealing at 400 ^oC. High-resolution transmission electron microscope (HRTEM) was adopted for microstructure analysis. Electrical characteristics, including capacitance-voltage (C-V), leakage current-voltage (I-V), and program/erase and retention behavior were also measured.

3. Results and Discussion

A cross-sectional HRTEM of the $SiO_2/W\text{-}ND/SiO_2/p\text{-}Si$ stacked structure without PDA is shown in Fig. 2. Spherical and separated W-NDs with diameters of 1.5~2 nm embedded in the silicon dioxide layer are clearly observed. The estimated density of W-ND is approximately $\sim 10^{13}$ cm^{-2} by HRTEM analysis.

To confirm memory operation, we measured the C-V characteristics with bi-directional voltages sweeping from 12 to –12 V and from –12 to 12 V for MOS capacitors with and without W-ND, as shown in Fig. 3. Considering that no hysterisis C-V behavior of MOS capacitor without W-ND, the larger counterclockwise hysterisis for W-ND MOS capacitors can be attributed to charge exchange between W-ND and silicon substrate. It is also obvious that the memory window of device with PDA becomes markedly larger than that of the device without PDA. We measured flat band voltages as a function of Program/Erase voltage for W-ND MOS capacitors with and without PDA, as shown in Fig. 4. We found that the program and erase operation started from Vg=±7V, and that the maximum memory window value was about 2.1V at Vg=±12V for the W-ND MOS capacitor without PDA. In comparison, the W-ND MOS capacitor with PDA can be programmed and erased from Vg=±4V, and the maximum memory window value about 9.2V is obtained at Vg=±12V, which is 4 times larger than that without PDA. This larger memory window can be attributed to the quality improvement of silicon dioxide around W-ND, which is confirmed by the leakage current characteristics. Fig. 5 shows that the leakage current remarkably decreases about 2 orders after PDA.

We have calculated electron density charged in W-NDs with formula in reference [3]. In case that the electron is charged at the first layer of W-ND near the silicon substrate, almost $1.4x10^{13}$ cm^{-2} electron is necessary to achieve the memory window of 9.2 V. The electron number of $1.4x10^{13}$ cm^{-2} is larger than the W-ND density, indicating that the multiple W-ND layers serve as the electron-charging region. We have compared the dot size, dot density, and memory window with reported metal dots in Table I. Our device shows the higher density, smaller size of W-ND and larger memory window.

To measure the program and erase characteristics of W-ND MOS capacitor with PDA, the gate pulse of ±12V with various pulse widths was used. The flat band voltages after single pulse performance are measured from the C-V scan at the small voltage region near the flat band voltage. As shown in Fig. 6, we found that the change of flat band voltage was about 3V after 1us program, and 10ms erase. The program speed is markedly faster than the erase one, which is due to different barrier heights for both electron injection and emission between W-ND and silicon substrate.

Fig. 7 shows the data retention characteristics of W-ND MOS memory device with PDA after program and erase at ±12V for 1s. As we observe, the larger memory window about 1.4V was remained at retention time of 10^5 s. To obtain the ten-years retention time, it is necessary to improve the retention characteristics of W-ND MOS memory device further.

4. Conclusions

MOS memory device with extremely high density ($1x10^{13}$ cm^{-2}) and small diameter (1.5~2nm) W-ND floating gate was fabricated. After 900 ^oC PDA, the extremely larger memory window about 9.2 V was obtained, indicating that it is a strong contender for future NVM applications. The program/erase speed and retention characteristics were evaluated also.

Acknowledgments

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References

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[2] M. Takata et al., IEDM Tech. Dig., pp. 22.5.1-22.5.4, 2003.
[3] H. I. Hanafi et al., IEEE TED-43, pp. 1553-1558, 1996.
[4] J. J. Lee et al., IEEE TED-52, pp. 507-511, 2005.

Table I. Comparison of metal nano-dot characteristics

Reported results	Metal nano-dot	Size (nm)	Density (/cm^2)	Memory window
Our work	W	1.5~2	1x10^{13}	9.2V
Samanta et al. [1]	W	5~10	<10^{12}	3.6V
Lee et al. [4]	Ni	5	5x10^{11}	1.5V
Takada et al. [2]	W	2~3	1x10^{13}	2.2V

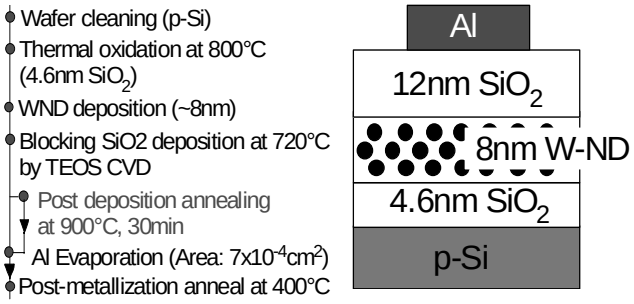

Fig. 1. Process flow and schematic cross-section of MOS capacitors with W-ND.

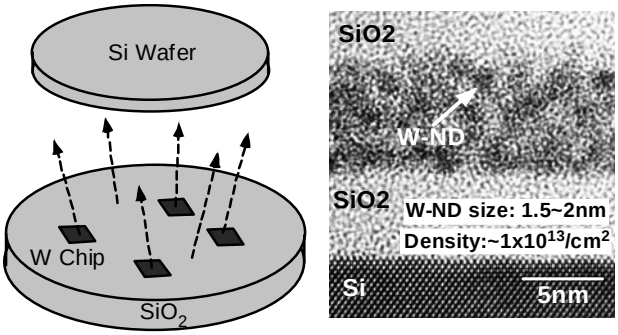

Fig. 2. Schematic of SAND method and HRTEM cross-sectional image of 8-nm-thick W-ND film formed on thermally oxidized silicon substrate without PDA.

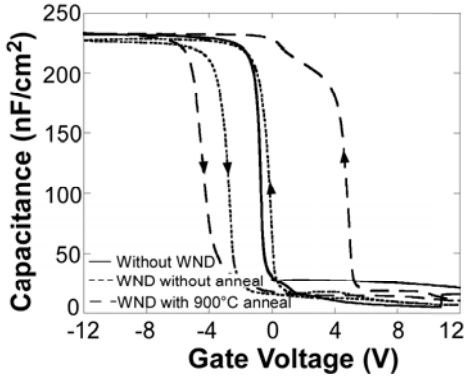

Fig. 3. C-V hysteresis curves for MOS capacitors with and without W-ND layer.

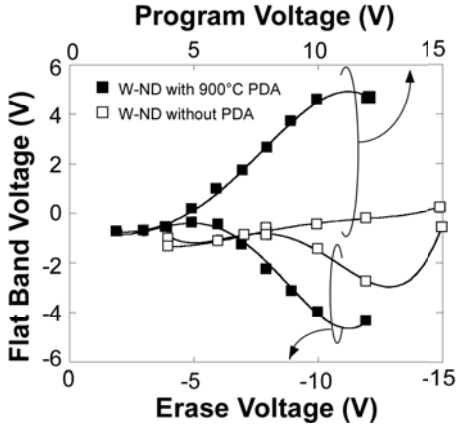

Fig. 4. Memory window as a function of Program/Erase voltage for W-ND MOS capacitors with and without PDA.

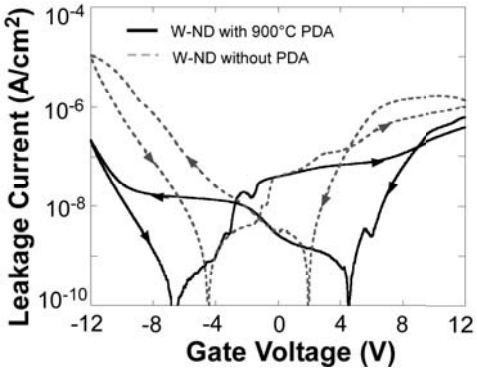

Fig. 5. Leakage current behaviors of W-ND MOS capacitors.

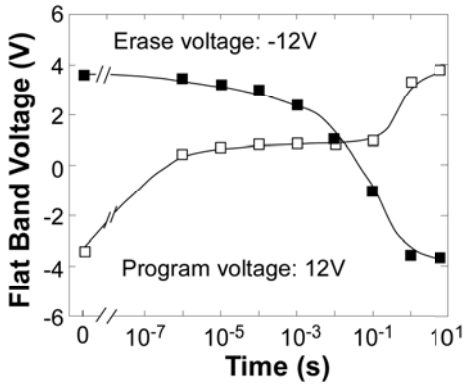

Fig. 6. Program/Erase speed characteristic of W-ND MOS capacitor with PDA at 900°C.

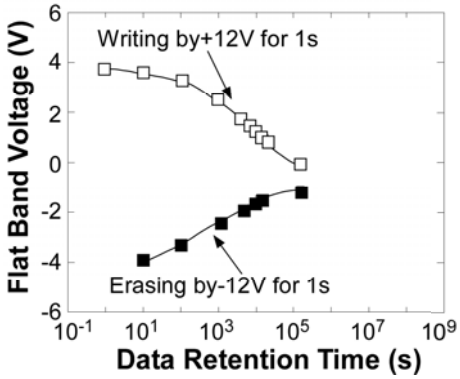

Fig. 7. Data retention characteristic of W-ND MOS capacitor with PDA at 900°C.