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2-bit/cell Characteristics of High-Density and High-Performance SONOS Flash Memory Cell with Recessed Channel Structure

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1. Introduction

Recently FinFET structure has been investigated to achieve high-density and high-performance SONOS flash memory cell transistors [1],[2]. However it is very difficult to implement 2-bit/cell in the memory cell based on FinFET and planar channel structures when the gate length scales down to sub-100 nm, because of charge redistribution problem [3]. To solve the charge redistribution problem, the nitride storage layer was formed separately on the source and the drain sides [4],[5] in sub-100 nm regime. However, scaling-down of these devices to 50 nm degrades significantly V_{th} sensing margin. In order to solve the problem, we have proposed a new flash memory cell which has nitride spacer for charge storage formed on the side-wall of recessed channel region [5], and shown programming characteristics with channel doping profile.

In this work, we propose a new cell transistor where the nitride layer for charge storage is formed on the whole recessed region. Device simulations are extensively performed to characterize hot-electron-injection (HEI) for a bit programming and hot-hole-injection (HHI) for a bit erasing. Various device characteristics are shown with channel doping profile.

2. Device Structure

Fig. 1 shows 2-D cross-sectional schematic view of the proposed device structure. The x_j stands for the junction depth from the top of the body and is fixed at 30 nm. The width (x_{rw}) and depth (x_{rd}) of the recess region are 50 nm and 100 nm, respectively. We call the recess width as the gate length (L_g), although actual effective channel length (($L_{eff}=\pi r+2(x_{rd}-x_j-r)$) is about 170 nm in this work. The physical control gate width is 20 nm for the given L_g of 50 nm. The thickness of O/N/O layers is 4/5/6 nm. We considered mainly three types of localized channel doping for reasonable 2-bit operation. The #1 channel doping of boron (peak: 1 ~ 3×10^{18} cm^{-3}) is localized nearby metallurgical S/D junction for V_{th} control, DIBL suppression, and hot electron generation. The #2 channel doping (n-type, peak=1~2×10^{18} cm^{-3}) is localized optionally near the bottom of recess region to relieve bottom corner effect. The device has #3 localized Gaussian boron doping (peak = 2×10^{18} cm^{-3} and ΔR_p= 82 nm) at 350 nm underneath from the top of the body to control body (or well) doping and field isolation V_{th} control.

3. Device Simulation and Results

Figs. 2 (a) and (b) show log I_D-V_{GS} characteristics of conventional planar channel SONOS device with L_gs of 160 and 50 nm, respectively, before and after programming by injecting channel hot electrons to the storage node. Programming time (t_{PGM}) is 1 μs with V_{GS}=5 V and V_{DS}=3.5 V. The V_{th} shift (ΔV_{th}) in 160 nm device is about 2 V for a given V_{DS}=0.1 V. The V_{th} margin for 2-bit/cell operation at a given read bias of 1.5 V is about 1.94 V. This 160 nm device shows not only good 2-bit operation but also good DIBL (32.2 mV/V) characteristics. However, ΔV_{th} and V_{th} margin of 50 nm device are about 4 V and 1.47V, respectively. High ΔV_{th} is due to fixed program bias at greatly reduced L_g. Those characteristics look good for 2-bit/cell operation, but the 2-bit/cell operation is impossible if we consider charge redistribution with temperature. This device has very poor DIBL (1.3 V/V), which probably makes impossible multi-level cell operation.

Fig. 3 shows ΔV_{th} and V_{th} margin from reported 80 nm device structure as shown in the insert [4]. Device characteristics for 2-bit/cell operation are not so good, and seem to be degraded with decreasing L_g.

Figs. 4 and 5 show log I_D-V_{GS} characteristics and the V_{th} of the proposed device with only #1 and #3 doping profiles, respectively. We achieved V_{th} margin of 0.53 V which is very poor. In Fig. 5, the ΔV_{th} for a #1 peak doping (N_{Apeak}) of 1×10^{18} cm^{-3} increases slightly with the ΔR_p due to the increase of field intensity. For higher #1 N_{Apeak}s than 1×10^{18} cm^{-3}, ΔV_{th} and V_{th} margin decrease because the V_{th} near the bottom of the recess region is increased by ΔR_p increase.

Fig. 6 shows log I_D-V_{GS} characteristics of the proposed device with the counter doping near the bottom region by applying n-type doping (peak=1.5×10^{18} cm^{-3} and ΔR_p =15 nm). The n-type doping alleviates significantly the V_{th} shift by the unwanted charge trapping near the bottom of the recess region. As a result, V_{th} margin was significantly improved to 2.23 V.

Fig. 7 shows ΔV_{th} and V_{th} margin with the ΔR_p of #1 p-type doping profile when the device has the counter doping near the bottom of the recess region. With increasing ΔR_p, ΔV_{th} and V_{th} margin are improved generally. As the #1 N_{Apeak} increases, ΔV_{th} and V_{th} margin are also improved. The device with the #1 N_{Apeak} of 3×10^{18} cm^{-3} shows improved results for small ΔR_p, but reduced improvement for further increase of ΔR_p because the V_{th} near the bottom corner is affected.

In Fig. 8, shown are ΔV_{th} and V_{th} margin with the ΔR_p of #2 n-type doping profile. Figure (a) and (b) show the data for the #1 N_{Apeak}s of 1 and 2×10^{18} cm^{-3}, respectively. As the ΔR_p of #2 n-type doping increases, the ΔV_{th} decreases due to reduced peak electric filed near x_j. V_{th} margin increases at first and then decreases since there is a trade-off exists between the alleviation of bottom corner effect and reduced peak electric filed near x_j.

Fig. 9 shows V_{th} behaviors versus drain voltage (V_D) for bit-erasing by HHI as a parameter of easing time (t_{ERS}: 0.1 and 0.5 μs) at a fixed V_G of -5 V. The doping profiles are the same as shown in Fig. 6. Erasing speed is improved greatly by increasing V_D to 6 V.

4. Conclusion

We have proposed 2-bit/cell SONOS flash memory devices with nitride charge trapping layer in recessed channel region for sub-50nm technology. By controlling the channel doping profiles in terms of peak concentration, ΔR_p, and doping type, we achieved successfully 2-bit/cell operation with a V_{th} margin larger than ~2 V and good erasing speed characteristics at a given gate length of 50 nm.

Acknowledgement

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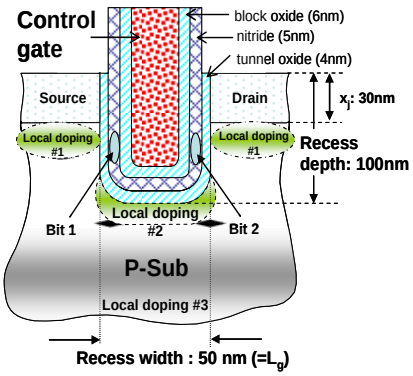
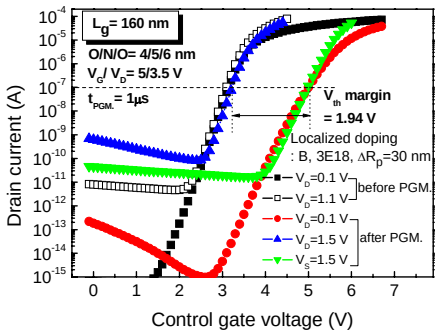
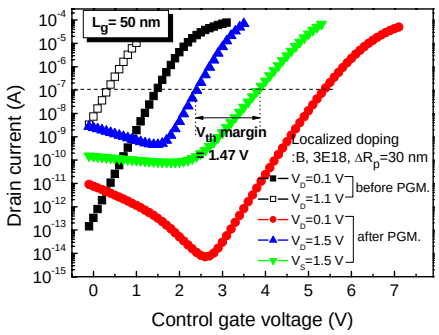


Fig. 1. 2-D cross-sectional schematic view of the proposed device structure. The x_{rd} and x_{rw} are fixed at 50 and 100 nm, respectively.



(a)



(b)

Fig. 2. *log* I_D-V_G characteristics of conventional planar devices with L_gs of 160 nm (a) and 50 nm (b), before and after programming by channel HEI. The devices have localized channel doping profile (peak= 3×10^{18} cm^{-3} and ΔR_p= 30 nm).

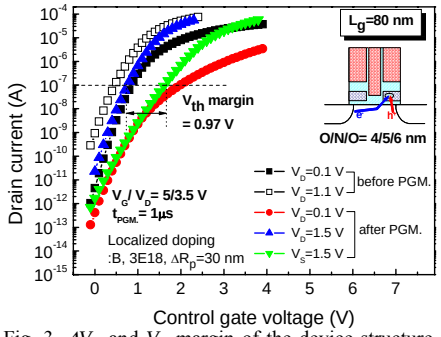


Fig. 3. ΔV_{th} and V_{th} margin of the device structure reported by B. Y. Choi et al [4]. The L_g is 80 nm. For a fair comparison as possible, similar channel doping profile was applied.

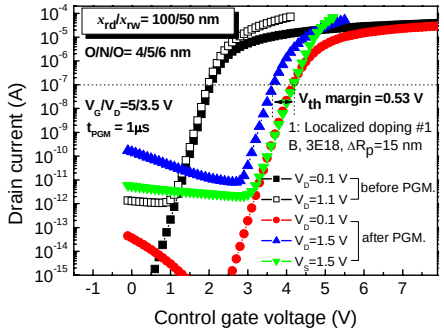


Fig. 4. *log* I_D-V_G characteristics of proposed device with only #1 and #3 local doping profiles, before and after programming by HEI.

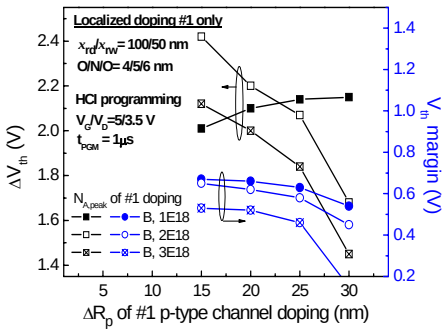


Fig. 5. ΔV_{th} and V_{th} margin of proposed devices versus ΔR_p of #1 p-type channel doping profile. The devices have only #1 and #3 doping profiles.

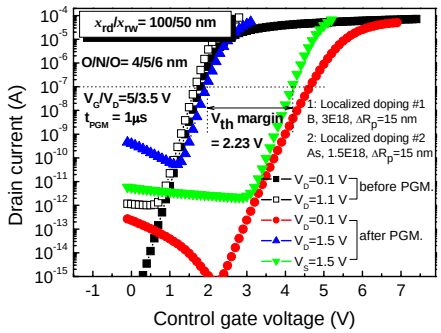


Fig. 6. *log* I_D-V_G characteristics of proposed device with #1, #2 and #3 local doping profiles, before and after programming by HEI.

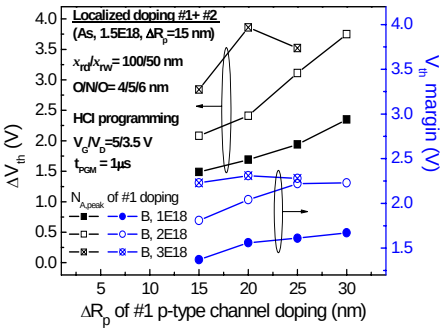
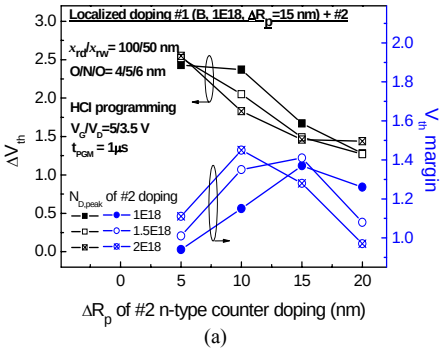
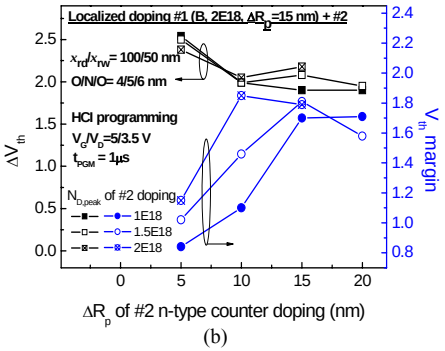


Fig. 7. ΔV_{th} and V_{th} margin of programmed devices with the counter doping near the bottom versus ΔR_p of p-type channel doping profile as a parameter of p-type peak doping concentration.



(a)



(b)

Fig. 8. ΔV_{th} and V_{th} margin versus ΔR_p of #2 n-type doping profile. Peak #2 doping concentrations are 1×10^{18} cm^{-3} (a) and 2×10^{18} cm^{-3} (b), respectively.

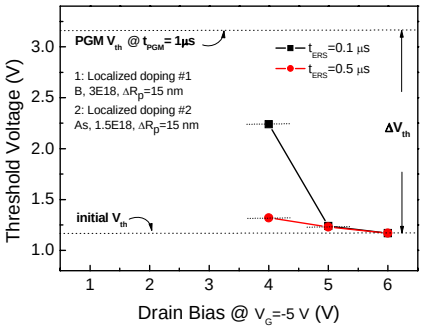


Fig. 9. V_{th} characteristics versus V_D as a parameter of easing time (t_{ERS}: 0.1 and 0.5 μs) at a fixed V_G of -5 V. The single bit-erasing is obtained by HHI.