Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 322-323

J-3-4

Ramping Amplitude Multi-Frequency Charge Pumping Technique for Silicon-Oxide-Nirtride-Oxide-Silicon Flash EEPROM Cell Transistors

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1. Introduction

Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) flash memory has recently received much interest for future nonvolatile memory devices in nano-electronics due to their smaller size and simpler process integration. Contrary to the floating gate flash memory where charge is uniformly stored in the floating gate, SONOS cell transistors have a nitride on top of the tunnel oxide and the charge is locally trapped during programming and erasing through the tunnel oxide. Therefore, to evaluate the trapping properties of the nitride layer is very important for understanding the charge trapping memory devices including charge loss and retention mechanisms. Up to the present, however, the study for these points is not enough. Previously reported characterization methods are based on the comparison of the subthreshold characteristic with carefully calibrated 2-D simulations [1], or the low frequency charge pumping measurement [2]. These methods are complicate or limited to thin tunnel oxide.

In this study, we have firstly proposed a new charge pumping technique, ramping amplitude multi-frequency charge pumping, to analyze trap characteristics of SONOS cell transistors and extracted each trap parameters in the nitride layer as well as the tunnel-oxide/Si interface respectively based on the new method.

2. Device structure and Experiments

The device structure for experiments is n-channel Silicon-Oxide-Nitride-Oxide-Silicon transistor with total gate area of 6 um^2 and gate dielectric stacks are consisted of Al_2O_3 blocking-oxide, nitride layer, and tunnel-oxide, respectively.

The setup for the charge pumping measurement is described as follows; a pulse train from a pulse generator (Agilent 41501B) was applied to the gate of the n-channel SONOS cell; the rise and fall times of the square wave were held at a constant value of 100 ns; the frequency of gate pulses applied in this paper is in the range of 100 KHz–500 KHz. The corresponding charge pumping currents (I_{CP}) were measured using a semiconductor parameter analyzer (Agilent 4156C). To investigate traps at various locations in ONO structure, a CP technique with gate pulses of fixed base level and ramping amplitude was employed.

3. Results and discussion

Fig. 1 shows the measurement results of I_{CP} as a function of rising/falling time (Fig. 1(a)) in SONOS cell transistors with mean trap density and capture cross section (Fig. 1(b)). This method is conventional technique limited to SiO_2/Si interface. Fig. 2 shows the oxide trap density evaluated by the conventional charge pumping technique for oxide trap profile [2]. But detecting range is within ~12Å from SiO_2/Si interface as shown Fig. 2. Therefore, it is needed to develop new charge pumping method for applying to SONOS cell transistors to find trap characteristics in nitride layer.

Fig. 3(a) shows the measurement results of I_{CP} from the proposed ramping amplitude multi-frequency charge pumping method. As the gate pulse high level (V_h) increases, more carriers can tunnel through the tunnel oxide with longer time to recombine with trapped carriers in nitride layer showing second peak in dI_{cp}/dV_h as shown in Fig. 3(b), which means inner traps of charge trapping layer can be evaluated. In Fig. 4, the proposed new model for SONOS cell is illustrated with schematic diagram for the locations of charge traps. As stated in [3], the total traps (N_t) involved with SONOS cell can be divided into two parts. One is tunnel-oxide/Si interface traps (N_{it}) and the other is inner traps of ONO, which can be classified into tunnel-oxide/nitride (N_{TN}), nitride bulk (N_N), and blocking-oxide/nitride (N_{BN}). In the case of the capture cross sections, it is possible to extract them by comparing the model with experimental data and using the measured gate current as shown in Fig. 5 even if the time constants of each traps are different. Fig. 6 shows N_t as a function of frequency at V_h=8 V which is enough large for inner traps to be evaluated. The trap parameters are extracted by fitting the proposed model to the experimental data and summarized in table I. The results are 3.76×10^{12} cm^{-2} for N_{TN}, 1.8×10^{12} cm^{-2} for N_N, 1.93×10^{11} cm^{-2} for N_{BN}, and 5.85×10^{12} cm^{-2} for total trap density including tunnel-oxide/Si. Trap density calculated by charge pumping current is consistent with trap density calculated by IV measurement as shown in Fig. 7. For the capture cross-section, the extracted values are 6.53×10^{-12} for σ_{TN}, 9.14×10^{-12} cm^2 for σ_N, and 1.83×10^{-13} cm^2 for σ_{BN}. These capture cross sections are effective capture cross section at each trap location. Its values are slightly larger than reported values at previous work due to the differences of the gate leakage current magnitude and charge trapping characteristics of nitride layer [4].

4. Conclusions

We firstly proposed a new charge pumping technique for SONOS cell transistors to characterize various inner traps in ONO structure. Using ramping amplitude multi-frequency charge pumping technique, we could extract trap density and capture cross-section at tunnel-oxide/nitride interface, nitride bulk, and blocking-oxide/nitride interface. We found that the total trap density is consistent with trap density calculated by IV measurement and capture cross section is slightly larger than reported values due to the gate leakage current magnitude and charge trapping characteristics of nitride layer.

Acknowledgements

This work is supported by Hynix semiconductor Inc.

References

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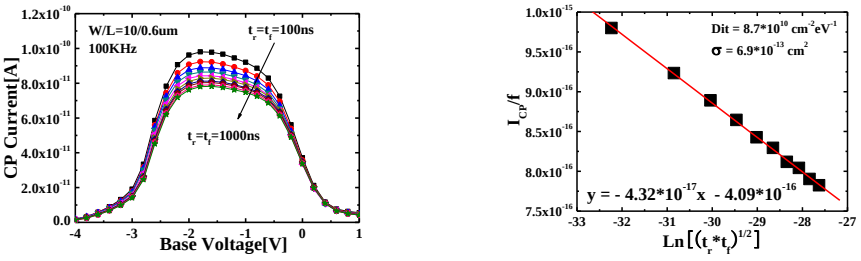


(a) (b)

Fig. 1 (a) Conventional measurement results of I_{cp} for different rising/falling times, (b) charge recombination (I_{CP}/f) as a function of Ln[$(t_r*t_f)^{1/2}$] provides tunnel-oxide/Si interface trap density (D_{it}) and mean capture cross section (б).

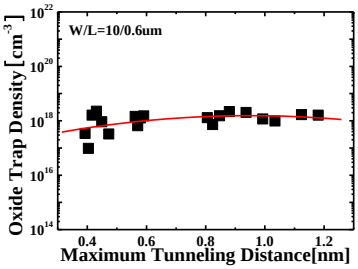
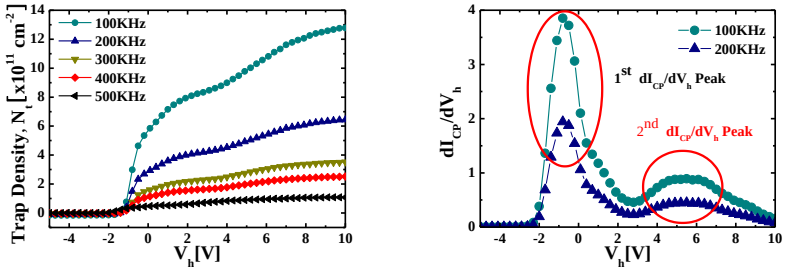
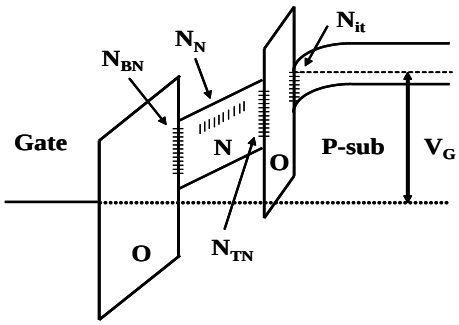


Fig. 2 Oxide trap density plotted as function of the maximum tunneling distance.



(a) (b)

Fig. 3 (a) Ramping amplitude multi-frequency charge pumping measurement. Base voltage was fixed as -12V, (b) Second peak for differentiation of I_{CP} is caused by recombination at trapping layer.



N_{it} : tunnel - oxide/substrate interface trap density

N_{ON} : tunnel - oxide/nitride interface trap density

N_N : nitride bulk trap

N_{BN} : blocking - oxide/nitride interface trap density

$$N_t = N_{it} + N_{TN}[1-\exp(-\frac{t}{\tau_{TN}})] + N_N[1-\exp(-\frac{t}{\tau_N})] + N_{BN}[1-\exp(-\frac{t}{\tau_{BN}})]$$

$$\tau_{TN} = \frac{q}{\sigma_{TN} J_G},\ \tau_N = \frac{q}{\sigma_N J_G},\ \tau_{BN} = \frac{q}{\sigma_{BN} J_G}$$

Fig. 4 Schematic diagram for the locations of charge traps and its modeling for SONOS cell transistors. Using this model the capture cross sections can be also evaluated with each trap density by using the gate current density.

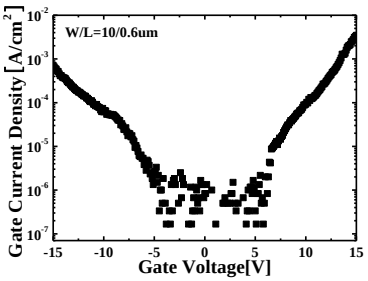


Fig. 5 gate current density of SONOS cell with total gate area of 6 um^2.

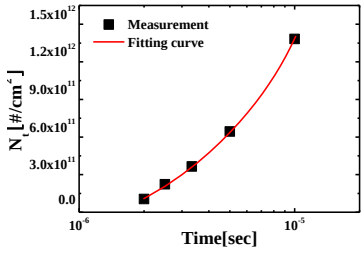


Table. 1 Summary of trap parameters extracted from the proposed model.

Trap density [#/cm^2]	N_{it}	9.74×10^{10}
	N_{TN}	3.76×10^{12}
	N_N	1.80×10^{12}
	N_{BN}	1.93×10^{11}
Capture Cross Section [cm^2]	σ_{it}	6.90×10^{-13}
	σ_{TN}	6.53×10^{-12}
	σ_N	9.14×10^{-12}
	σ_{BN}	1.83×10^{-13}

Fig. 6 Total trap density (N_t) as a function of frequency at V_h=8 V which is enough large for inner traps to be evaluated. The trap parameters are extracted from fitting the proposed model to experimental data.

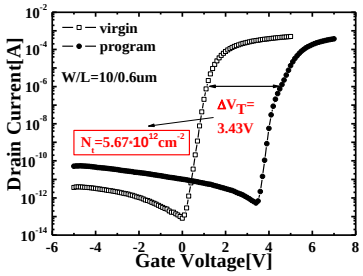


Fig. 7 Total trap density calculated by V_{TH} shift in IV curve.