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Current Status and Future View of Phase Change Memory

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1. Introduction

Recently, there has been a growing need for nonvolatile memories for devices such as mobile phones, automobiles, digital appliances. Phase-change memory (PCM) is a promising nonvolatile memory because of its large sensing margin, fast writing speed, high endurance, and long data retention time [1-3]. As it has a very simple structure, that is, only one transistor and one resistor, producing PCM is less expensive than other memories. Furthermore, its CMOS compatibility and scalability are preferable for use in both stand-alone and embedded applications.

The current status and research trends reported for PCM are discussed here, and, on the basis of the results in these reports, the future view of PCM is also discussed.

2. Current Status

The two key issues in current research are reducing programming power and scaling the cell area. Both are essential to develop the PCM that is easy to manufacture. The recent trends for each will be described below.

Conventional PCM needs a large programming current and a high voltage, especially in reset operation. In this process, the chalcogenide material is melted once by joule heating in order to form an amorphous state by rapid cooling. As doing this requires a large power supply, MOSFETs with a large gate width are needed to be used as a switching device. These transistors need a large circuit area. Therefore, to produce a CMOS-compatible PCM for embedded applications, decreasing both reset current and voltage is necessary. Reducing the reset current is also desirable for stand-alone applications because a small MOSFET is needed for high-density memory.

To decrease the programming power, several techniques have been proposed: first, miniaturizing the bottom electrode contact area, second, using a confined cell structure, third, modifying the GeSbTe materials, and fourth, utilizing the interfacial layer.

The benchmark measurements of the reset current are shown in Figure 1. The reset current of planar structure decreases with decreasing bottom-electrode contact area [6-8]. This is because the programmable volume of GeSbTe is shrunk by use of the bottom electrode with a small diameter. Therefore, even though doing so complicates the process, several techniques for making a smaller contact have been investigated [4,9,13,16]. These techniques make use of the fact that, as shown in Fig. 1, reset current decreases with contact area. However, it can be seen that the edge contact type [4] departs from this trend. Another effect for reducing current is thought to be included, such as attributable to the interface between GST and the bottom electrode.

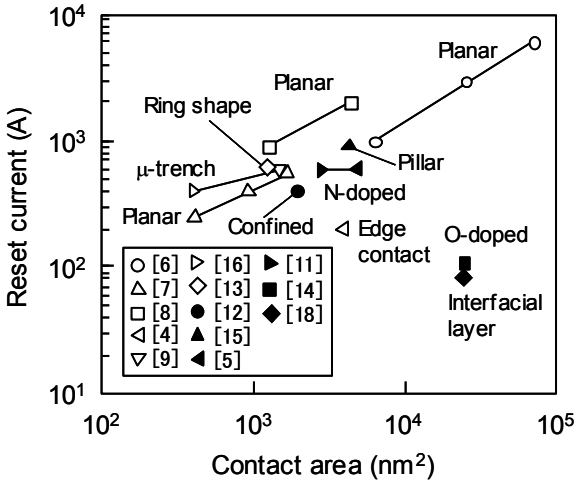

Figure 1. Reset current benchmark as a function of bottom-electrode contact area.

Also, as the confined structure makes the current more concentrated and decreases the effective programmable volume, the reset current reduces [12,15]. As shown in Fig. 1, we can confirm that the reset current is lower than that of the conventional planar structure.

Controlling the resistivity GeSbTe by doping also enables low power operation [5,11,14]. This is done with a simple process: the GeSbTe is prepared by sputtering using a mixture of N_2 or O_2 gas with Ar. As shown in Fig. 1, the oxygen-doped GeSbTe has significantly decreased the reset current [14]. In addition to the high resistance of Ge-O in GeSbTe materials, the heat isolation effect by the interfacial layer, which is described below, is probably included because the plug surface is oxidized by the mixed O_2 during sputtering.

The programming power for the cell is also reduced by inserting a very thin Ta_2O_5 film between the GeSbTe and the plug [18]. The Ta_2O_5 interfacial layer works as a heat

insulator, and thus enables heat to be effectively generated in GeSbTe.

The cell size should ideally be as small as possible, especially for those used in high-density memory. The trend of memory cell area is shown in Figure 2. It is clear that the scaling of the memory cell is developed by decreasing the design rule and unit cell size [9-11,13,16,17]. In addition, the switching device is changing from a MOSFET to a bipolar transistor and diode because their vertical and self-aligned cell structure [16,17] means that smaller cells are possible. The cell area is significantly decreased to about 10% in a few years. For latest technology devices that use $5.8F^2$ cells at the 90-nm design rule, the cell area reached 0.047 μm^2, which is equivalent to that of NOR flash memory [17].

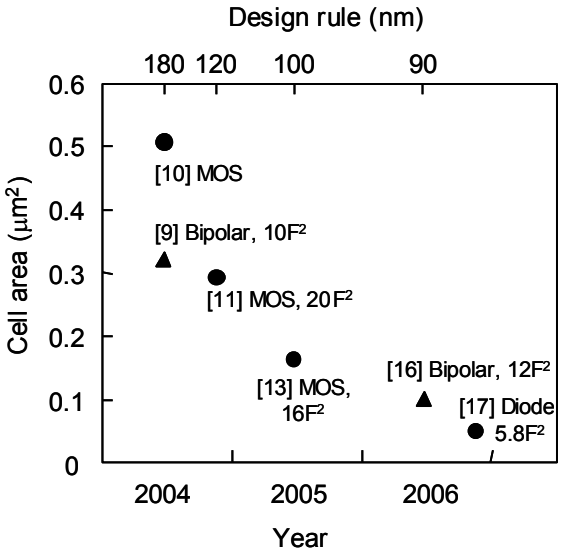

Figure 2. Trends in scaling of memory cells.

Although there are still some issues that relate to scaling, for example, thermal cross-talk between adjacent bits [7] and dry etching damage on the sidewall of GeSbTe [17], they are expected to be solved by optimizing of the insulator materials and improving the process conditions. We can state that there is appears to be no crucial difficulty that limits the scaling of memory cells.

3. Future View

Two important issues, reducing programming power and scaling the cell area, are in the process of being solved. The reset current can be reduced to a level for operation that is compatible with that of MOSFETs used in conventional CMOS technologies. Also, the memory cell area is as small as that of current NOR flash memory. These results indicate that PCM is nearly ready for use in practical applications.

Phase-change memory is suitable for use in both stand-alone and embedded applications. To be used in stand-alone applications, PCM needs to have small cells and high density. Therefore, a memory cell structure that uses scalable switching devices such as diodes, will need to be further developed. However, making such as structure requires a special process. On the other hand, if PCM is to be used in embedded applications, CMOS-compatible memory cells, which are operated with logic core MOSFETs, will have a small peripheral circuit area as well as a small memory cell area. Therefore, the most important issue is how to decrease both reset current and voltage. The target application is likely to determine where future developments take place: in the area of improving the density of memory cell structure or in the area of decreasing the reset current and voltage.

Also, before mass production begins, various issues to investigate remain, such as thermal retention characteristics, the degradation mechanism, and reliability.

4. Conclusion

Phase change memory is attracting increasing interest as a candidate for embedded and stand-alone applications. Research in the last few years has focused on the important issues involved in its practical application. As these issues are nearing a solution, the PCM will soon enter a rapidly growing market.

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References

[1] S. Lai et al., *IEDM Tech. Dig.* (2001) p.803.
[2] A. Pirovano et al., *IEDM Tech. Dig.* (2002) p.923.
[3] Y.N. Hwang et al., *Symp. on VLSI Tech. Dig.*, (2003) p.173.
[4] Y.H Ha et al., *Symp. on VLSI Tech. Dig.* (2003) p.175.
[5] H. Horii et al., *Symp. on VLSI Tech. Dig.*, (2003) p.177.
[6] S. Lai, *IEDM Tech. Dig.* (2003) p.255.
[7] A. Pirovano et al., *IEDM Tech. Dig.* (2003) p.699.
[8] Y.N. Hwang et al., *IEDM Tech. Dig.* (2003) 37.1.
[9] F. Pellizzer et al., *Symp. on VLSI Tech. Dig.* (2004) p.18.
[10] S.H. Lee et al., *Symp. on VLSI Tech. Dig.* (2004) p.20.
[11] S.J. Ahn et al., *IEDM Tech. Dig.* (2004) 9.7.
[12] S.L. Cho et al., *Symp. on VLSI Tech. Dig.* (2005) p.96.
[13] S.J. Ahn et al., *Symp. on VLSI Tech. Dig.* (2005) p.98.
[14] N. Matsuzaki et al., *IEDM Tech. Dig.* (2005) p.758.
[15] T. D. Happ et al., *Symp. on VLSI Tech. Dig.* (2006) p.148.
[16] F. Pellizzer et al., *Symp. on VLSI Tech. Dig.* (2006) p.150.
[17] J.H. Oh et al., *IEDM Tech. Dig.* (2006) p.49.
[18] Y. Matsui et al., *IEDM Tech. Dig.* (2006) p.769.