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Three-Dimensional Electro-Thermal Compact Model for Reset Operation of Phase Change Memories

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Abstract

A three-dimensional (3D) electro-thermal compact model for the reset operation of a phase change memory (PCM) cell is presented. This model takes into account three-dimensional spreading of heat flux and current flow which depend on the PCM cell structure. The interfacial thermal resistance, which has a crucial effect on the thermal conduction in a PCM cell, is also considered. The accuracy of the model is confirmed by comparing the simulation results with measurement.

1. Introduction

Chalcogenide-based phase change memory is one of the most promising candidates for the next generation non-volatile memory [1]. The reduction of programming current for reset operation, by which the chalcogenide turns into amorphous, is important for the low power operation. Therefore, an accurate model for the reset operation of a PCM cell is needed. While detailed numerical models were developed for PCM [2] [3], a physics-based analytical model is desired for fast evaluation of device operation.

In this work, we present a 3D electro-thermal model for the reset operation of a PCM cell. The validity of the model is confirmed by comparing the simulation results with measurement data. Finally, we discuss the scalability of PCM from the process fluctuation point of view.

2. Modeling

Thermal Model

Figure 1 shows (a) a typical PCM cell structure and (b) the thermal equivalent circuit. The heat generation occurred by the Joule heating can be assumed to be uniform along the interface between GST and the bottom electrode. This assumption is verified by comparing the temperature distribution obtained by the 2D device simulation (Fig. 2). In addition, based on this results, we describe the temperature contour in the GST layer as shown in Fig. 3. Thus, the 2D thermal resistance of the GST layer is given by

$$\begin{aligned} R_{\rm th}^{\rm GST} &= \frac{1}{k_{\rm GST}} \int_0^{t_{\rm GST}} \frac{dx}{2r+\pi x} \\ &= \frac{1}{\pi k_{\rm GST}} \log\left[\frac{\pi t_{\rm GST}}{2r}+1\right], \end{aligned} \quad (1)$$

where $k_{\rm GST}$ is the thermal conductivity of GST, $t_{\rm GST}$ is the thickness of the GST layer, $r = r_{\rm plug} + \Delta r$, $r_{\rm plug}$ is the radius of the bottom electrode and Δr is a parameter which expresses the spreading of the heat generation led by the multi-dimensional current flow and large electric field on the side edge of the bottom electrode. As shown in Fig. 4, $\Delta r = 15.3$ nm enables Eq. (1) to agree with the device simulation well. In the same way, the 3D thermal resistance of the GST layer is given by

$$\begin{aligned} R_{\rm th}^{\rm GST} &= \frac{1}{k_{\rm GST}} \int_0^{t_{\rm GST}} \frac{dx}{4r^2+4\pi r x+2\pi x^2} \\ &= \frac{1}{2\pi k_{\rm GST}(\alpha-\beta)} \log\left[\frac{\beta(t_{\rm GST}-\alpha)}{\alpha(t_{\rm GST}-\beta)}\right], \end{aligned} \quad (2)$$

where $\alpha = -r + r\sqrt{1-2/\pi}$ and $\beta = -r - r\sqrt{1-2/\pi}$.

Electrical Model

The $I-V$ characteristics of GST can be explained by the trap conduction model. The current flow due to carrier transport among traps is described as follows [4]:

$$I = 2qn\frac{\Delta z}{\tau} A \sinh\left(\frac{q}{k_B T}\frac{\Delta z}{2u_{\rm a}} V\right), \quad (3)$$

where q is the elementary charge, k_B is the Boltzman constant, n is the carrier concentration under zero bias, Δz is the average inter-trap distance, τ is the life time of the trapped carrier, T is the temperature, $u_{\rm a}$ is the thickness of the amorphous layer and A is the cross-sectional area. In order to take into account the 3D effect, A is described as a function of u_a:

$$A(u_{\rm a}) = \frac{2}{3}\pi u_{\rm a}^2 + 2\pi r u_a + 4r^2. \quad (4)$$

This model can be applied to the set state by replacing $u_{\rm a}$ by $t_{\rm GST}$. Fairy good agreements with measurement are obtained as shown in Fig. 5.

3. Results and Discussion

To confirm the validity of the proposed model, the reset operation of a PCM cell was simulated and the result was compared with the measurement presented in Ref. [5].

A typical dimension of the standard PCM cell is the order of submicrometer. Heat conduction at these scales can be strongly influenced by the interface thermal resistance $R_{\rm th}^{\rm Int}$, which is the order of 10^{-8} Km^2/W [6] [7]. Figure 6 shows the maximum temperature of the GST layer as a function of $I_{\rm bl}$. It is observed that the temperature rise of the GST layer was not enough for the reset operation without $R_{\rm th}^{\rm Int}$, which shows the importance to consider the $R_{\rm th}^{\rm Int}$. Furthermore, it is also observed that the Ta_2O_5 interfacial layer is significantly effective to raise the temperature, which enables low current reset operation. In addition, good agreements are observed between the measured and simulated reset currents in both

cases with and without Ta_2O_5. This confirms the validity of the proposed 3D electro-thermal model.

Finally, we estimated the effect of the process fluctuation to a reset operation. Figure 7 shows resistance variation caused by $r_{\rm plug}$ fluctuation after reset operation. The resistance varies by 20% when $r_{\rm plug}$ fluctuates by 5%. This indicates that the fluctuation of the plug radius would become one of the key issues to limit the scaling.

4. Conclusion

A 3D electro-thermal compact model for a PCM cell was presented. The validity of the model was confirmed by leading a good agreement to the measurement. In addition, it was pointed out that the fluctuation of the plug radius would become one of the key issues to limit the scaling of PCM.

References

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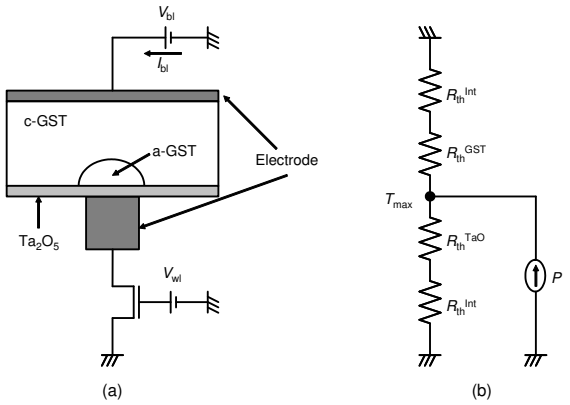

Fig. 1. (a) A typical PCM cell structure simulated in this study. (b) The thermal equivalent circuit of a PCM cell.

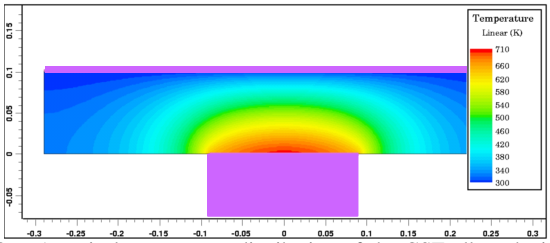

Fig. 2. A typical temperature distribution of the GST alloy obtained by the device simulation.

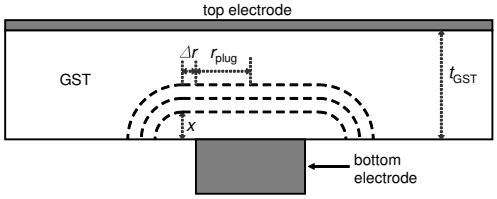

Fig. 3. The temperature contour of the GST layer considered in this study.

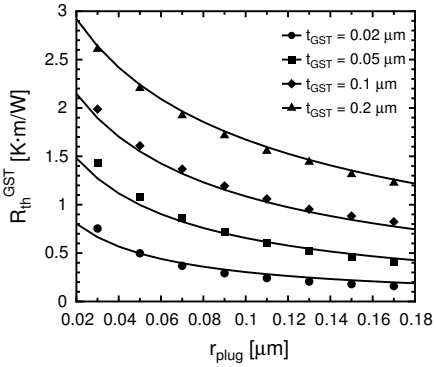

Fig. 4. The thermal resistance $R_{\rm th}^{\rm GST}$ as a function of the plug radius $r_{\rm plug}$. Symbols are the results of device simulation and lines are the data obtained by Eq. (1).

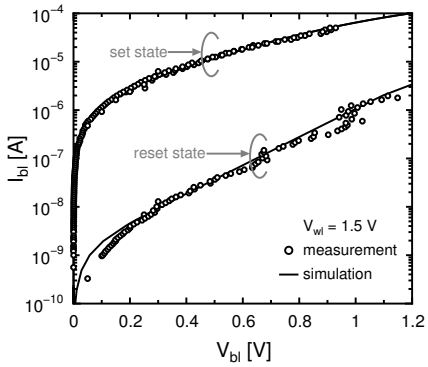

Fig. 5. Measured and simulated current-voltage characteristics of the PCM cell.

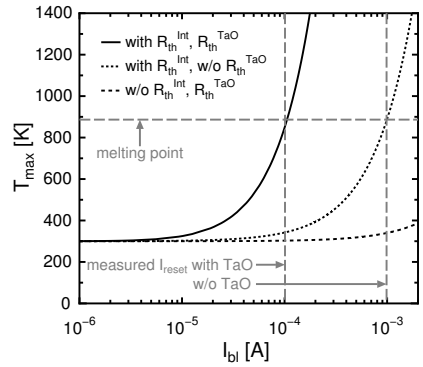

Fig. 6. The maximum temperature $T_{\rm max}$ in the GST layer as a function of the bit-line current $I_{\rm bl}$ with and without the interface thermal resistance $R_{\rm th}^{\rm Int}$ and the thermal resistance of the Ta_2O_5 layer $R_{\rm th}^{\rm TaO}$. $T_{\rm max}$ increases to the melting point of the GST when $I_{\rm bl}$ reaches the measured reset currents reported in Ref. [5].

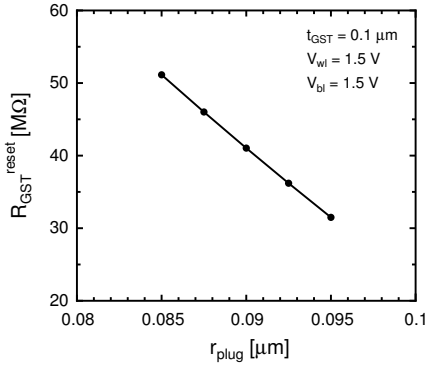

Fig. 7. The resistance of the GST $R_{\rm GST}$ after reset operation as a function of the plug radius $r_{\rm plug}$.