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Comprehensive HSPICE Model of Phase Change Memory Cell for Static and Transient Programming

Der-Sheng Chao[1, 2], Yan-Kai Chen[3], Yi-Bo Liao[3], Meng-Hsueh Chiang[3], Chenhsin Lien[2], Ming-Jer Kao[1], Ming-Jinn Tsai[1]

[1]Electronics and Optoelectronics Research Laboratories (EOL), ITRI
195, Sec.4, Chung Hsing Rd., Chutung, Hsinchu, Taiwan 310, R.O.C.
Phone: +886-3-5914350 E-mail: DSChao@itri.org.tw
[2]Institute of Electronics Engineering, National Tsing Hua University, Taiwan, R.O.C.
[3]Department of Electronic Engineering, National Ilan University, Taiwan, R.O.C.

1. Introduction

With increasing scaling difficulties of Flash memory in recent years, Phase Change Memory (PCM) has been considered the most promising candidate for the next generation nonvolatile semiconductor memory due to the competitive merits of fast speed, low power, good reliability, process compatibility with CMOS technology, and high scalability. Some works also demonstrated the high performance and superior manufacturability of PCM memory chip, indicating a great commercializing potential of PCM technology [1-3]. To prepare the advent of PCM production, establishing some feasible auxiliary tools is necessary to reinforce the driving capability and reduce the impact of commercialization, especially for a correct and flexible behavioral model which allows the electronic designers to facilitate the circuit design work. For this reason, this work proposes a comprehensive parameterized HSPICE model to approximate the programming behaviors of PCM cell. Based on this model, the static and transient responses for the reading and writing programming can be accurately simulated.

2. Cell Behaviors and Model Descriptions

The binary data storage in a PCM cell is accomplished by a fast and reversible phase transition between amorphous and crystalline phase in an active region of chalcogenide material, usually $Ge_2Sb_2Te_5$ (GST), which is thermally induced by Joule heating of current pulse to compose the high resistive RESET state and low resistive SET state. The RESET current pulse with a higher amplitude and shorter width is used to melt the GST alloy and rapidly quench. On the other hand, the SET current pulse has a lower amplitude and longer time so that it can crystallize the GST alloy with a sufficient time.

To extract the specific parameters corresponding to the cell characteristics for the circuit model, a novel PCM cell with double-confinement structure as shown in Fig. 1 was characterized [4]. As can be seen, the double confined cell has an additional bottom GST layer to effectively prevent the heat loss, so that the thermal efficiency is greatly improved and the programming current and power consumption are reduced. Fig. 2 shows the experimental I-V curves of SET state and RESET state for the double confined cell. In addition to the low-field steady states, the high-field I-V characteristics corresponding to the dynamic-on state can also be observed. In particular, an obvious threshold switching behavior for the RESET state and an intrinsic holding voltage can also be recognized. The programming current as well as the corresponding cell resistance for the double confined cell can be obtained from the typical R-I curve as shown in Fig. 3. To totally determine the cell characteristics, some specific parameters are selected to be considered in this circuit model as summarized in Table 1.

Figure 4 shows the circuit block diagram for the parameterized PCM HSPICE model proposed in this work. As can be seen, several dependent functional circuits used to describe the specific cell behaviors are included into a two-terminal HSPICE model. The input/output circuit uses the voltage controlled resistor (VCR) to determine the state of PCM cell (R_{RESET}, R_{SET}, or R_{on}). The constant voltage shift circuit as shown in Fig. 5 is also connected in the input/output circuit to behave the intrinsic holding voltage. To define the minimum induction times for amorphization and crystallization, the pulse width decision circuit is constructed on the basis of the RC integral circuit. Afterwards, the storage and data selection circuits are created to determine which state is stored according to the conditions of input pulse and then return the data to the input/output circuit.

3. Simulation Results

To demonstrate the correctness of the PCM HSPICE model, the testing circuit was set up as shown in Fig. 6, which is similar to the measurement setup used to characterize the double confined cell. The values of the specific parameters included in the model are also listed in Table 1. As shown, the input voltage pulse was applied to the PCM cell connected in series with a sense resistor of 2 kΩ, allowing extracting programming current and sensing cell resistance. Fig. 7 shows the transient response of the input voltage (V1) and the PCM voltage (V2). A sequence of input voltage pulses with a fixed pulse width of 50 ns and a gradual increase in amplitude from 0.2 to 4.1 V were applied to simulate the programming behaviors of PCM cell. The value of the parameter of initial condition (IC) for the model is set as 1 to indicate that the initial state is RESET state. Clearly, an abrupt drop in the PCM voltage occurs as the input voltage is higher than 0.8 V. This reveals that the threshold switching behavior can be well emulated by this model. On the other hand, Fig. 8 shows the history of the programming current (I_{PCM}) and the corresponding static cell resistance (R_{PCM}). As can be seen, the threshold switching causes an obvious increase in programming current so that the cell resistance is changed to the SET state. As the current increases further above the RESET current, the resistance again returns to the RESET state. Relying on this flexible model with some specific parameters, the simulated I_{PCM}-V_{PCM} and R_{PCM}-I_{PCM} curves for the double confined cell can be obtained as shown in Fig. 9 and Fig. 10. Clearly, the simulated behaviors are very analogous to the experimental results as shown in Fig. 2 and Fig. 3, implying the feasibility and correctness of this model.

It is worth to note that the programming dynamics during the threshold switching can be analyzed by this model. Fig. 11 (a) and (b) respectively show the simulated parasitic capacitance effect on the transient response of voltage and current during the threshold switching for the external parasitic capacitances (Cp) of 0 pF and 4 pF. As can be seen, the parasitic capacitance causes a current overshoot as the voltage suddenly drops after the threshold switching. This transient current overshoot may cause the parasitic RESET programming and affect the final phase distribution in the active region of PCM cell [5]. Therefore, it is important to perform the transient analysis using an accurate model for the PCM cell, especially when the cells are integrated into a memory array with periphery circuits.

4. Conclusions

This work proposes a comprehensive parameterized HSPICE model which can accurately simulate the programming behaviors of PCM cell. The two-terminal model can totally describe the specific cell behaviors by integrating several dependent functional circuits and including some specific parameters extracted from a novel double confined cell. The simulation results show that this model can display analogous static characteristics and transient behaviors to the experimental results. Therefore, this PCM HSPICE model can provide a correct mirror of the cell behaviors and is applicable to PCM chip design.

References

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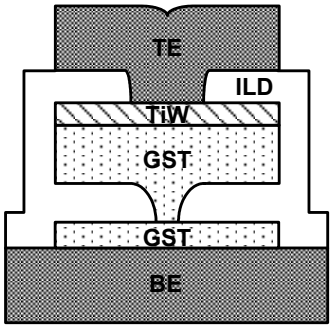

Fig. 1 Schematic cross section of double confined cell

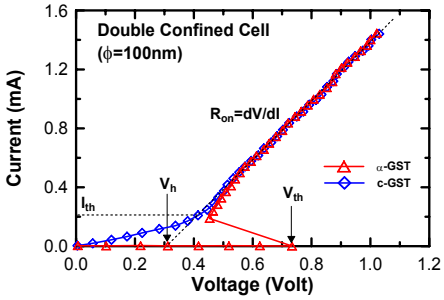

Fig. 2 Measured I-V curves for the double confined cell

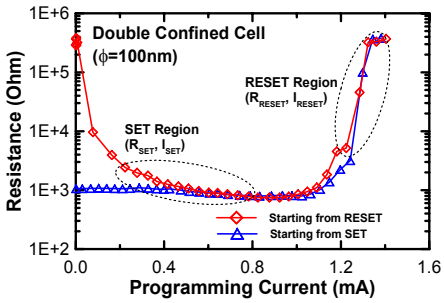

Fig. 3 Measured R-I curves for the double confined cell

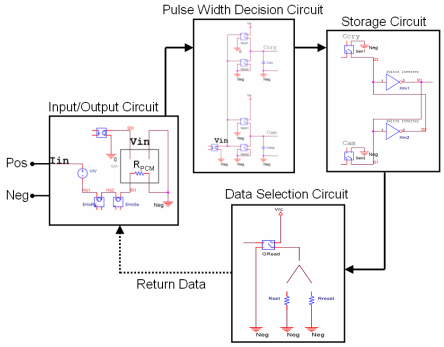

Fig. 4 Circuit block diagram for the parameterized PCM HSPICE model

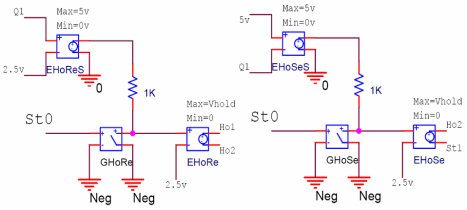

Fig. 5 Constant voltage shift circuit used to behave the intrinsic holding voltage

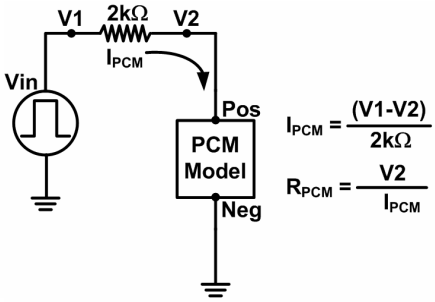

Fig. 6 Schematic view of testing circuit used to evaluate the PCM model

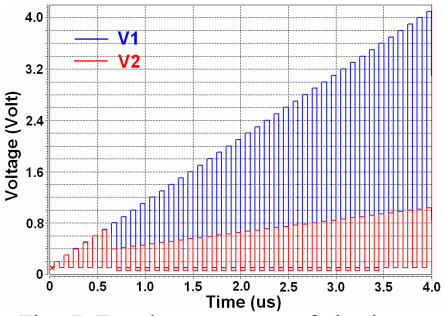

Fig. 7 Transient response of the input voltage (V1) and the PCM voltage (V2)

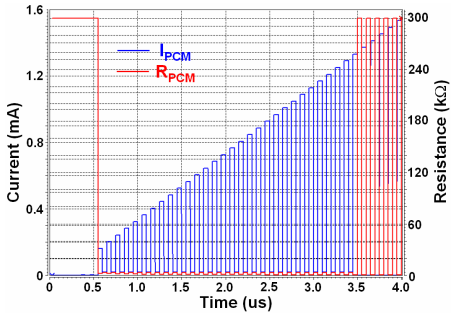

Fig. 8 History of the programming current (I_{PCM}) and the cell resistance (R_{PCM})

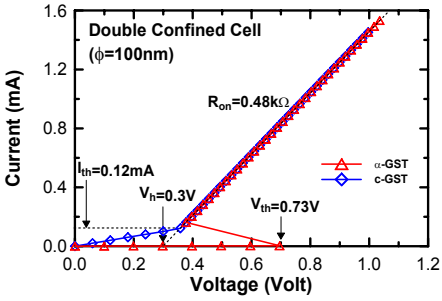

Fig. 9 Simulated I-V curves for the double confined cell by the model

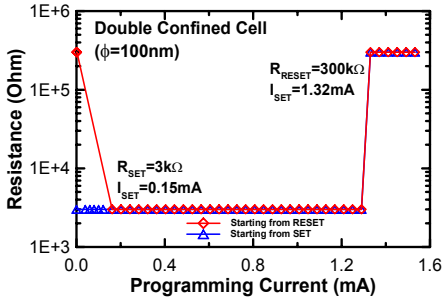

Fig. 10 Simulated R-I curves for the double confined cell by the model

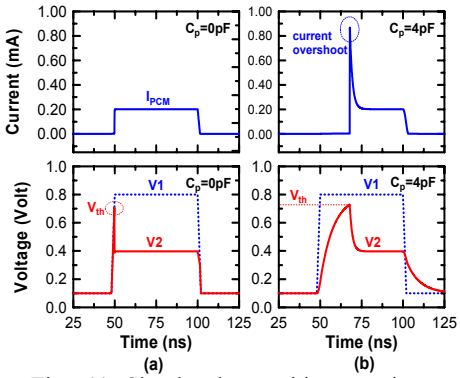

Fig. 11 Simulated parasitic capacitance effect on the programming transient during the threshold switching for (a) Cp=0 pF and (b) Cp=4 pF

Table 1 Summarized specific parameters included in this model

Parameter Description	Symbol	Value
RESET Resistance (kΩ)	R_{RESET}	300
SET Resistance (kΩ)	R_{SET}	3
Dynamic-on Resistance (kΩ)	R_{on}	0.48
RESET Current (mA)	I_{RESET}	1.32
SET Current (mA)	I_{SET}	0.15
Threshold Current (μA)	I_{th}	120
Threshold Switching Voltage (Volt)	V_{th}	0.73
Holding Voltage (Volt)	V_h	0.3
Minimum RESET Pulse Width (ns)	t_{RESET}	50
Minimum SET Pulse Width (ns)	t_{SET}	50
Initial Condition (1 for RESET & 0 for SET)	IC	0 or 1