Current Development Status and Future Challenge of Metal Oxide RRAM Technologies

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1. Introduction
Over the last seven or eight years, RRAM has emerged as the latest candidate for “next generation” nonvolatile memory [1]-[4], even though initial research on electrically induced resistance change was done as far back as the 1960’s [5]-[7]. Within this context, RRAM is discussed as “insulator resistance change memory” in the chapter of “Emerging Research Device” of 2005 ITRS in which the committee’s opinion regarding this technology is stated as follows, “If this effect can be controlled, memories based on this bi-stable switching process can be scaled to very low feature sizes. The switching speed is limited by ion transport. If the active distance that is relevant for the redox controlled bi-stable switching is small the switching time can be as low as a few nanoseconds. Precise predictions are not yet possible, because the details of the mechanism of the reported phenomena are still unknown.” [8]

Recently, the level of R&D effort directed toward RRAM has risen significantly, although other new memories are also under development for practical use. This is motivated by the realization that RRAM has the potential to surpass flash memory both in increased performance and reduced cost. In particular, both SET and the RESET operations can be performed by use of low voltage pulses of less than 50ns duration. Moreover, these electrical properties should allow RRAM to be used for rapid data download and storage of rich content as well as the flexibility of random rewrite of any individual byte. Furthermore, RRAM manufacturing is compatible with standard CMOS fabrication, requiring no additional specialized equipment, and has the possibility of 3D integration. [9] This paper will explore the present state of knowledge regarding the switching mechanism of RRAM and also discuss technical challenges in the current stage of development.

2. Operating Mechanism
Various metal oxide films exhibit semiconductor characteristics in which oxygen or metal defects act as donors or acceptors[7], [10]. Accordingly, resistance change phenomena caused by electric voltage pulses are frequently observed for both n-type metal oxides such as Ti and Ta and p-type oxides such as Ni, Co, and Cu. Selected data reported previously appears in Table 1. Resistance change from high to low value is thought to be due to defect generation and migration occurring when an electric field applied to a metal oxide film exceeds a particular threshold value [11]. This is supported by experiment and can explain the high switching speed of RRAM [12], [13]. However, several papers assert that such resistance changes are not uniform and occur locally through filamentary paths [4], [14], [15]. Indeed, such filaments are actually observed when the area of the electrode is large [16]. Of course, the area of any one filament is quite small and it is not clear what kind of electrical properties should be observed if device and filament sizes become essentially the same. On the other hand, resistance change from low to high value is believed to be caused by the flow of current above some threshold value. Presumably, this change corresponds to the disappearance of defects resulting from Joule heating [17], [18]. Indeed, current densities required for this process are similar to those of PCRAM. Thus, it is thought that an RRAM device is heated to a similar temperature as for PCRAM, and it may be further supposed that defect recovery occurs at very high speed.

Naturally, resistance change is thought to occur in the neighborhood of the electrode because observed effects of various electrode materials on RRAM electrical characteristics are significant. For instance, resistance switching is observed in a sample of titanium oxide in contact with a TiN electrode, but if a Ti metal electrode is used instead, observed IV characteristics are ohmic. In addition, in a state of high resistance, IV characteristics are strongly non-linear [19] and the temperature dependence of resistance is also comparatively large. In contrast, in a state of low resistance, observed IV characteristics are only weakly non-linear and temperature dependence is small.

3. Resistance switching mode of RRAM
Previous papers have reported two modes of RRAM resistance change, namely, bipolar and unipolar. In the case of bipolar mode, device resistance is controlled by electric pulses of different voltage polarity. Hence, both SET and RESET can be done at high speed (less than 50ns). In the case of unipolar mode, resistance is controlled by changing the duration of electric pulses of the same polarity. Accordingly, RESET takes more than ten longer than SET. Even so, we have found that these two reported switching modes can be explained by a unified model [20]. Moreover, based on this model new conditions have been found for which both SET and RESET can be achieved by 50ns pulses of the same polarity.
Clearly, programming and erasing of data can be done with low voltage, but some authors report that a so-called forming process using "ignition" pulses of higher voltage is required for initial resistance change [18]. However, our experimental results indicate that for an optimized device configuration, forming is unnecessary [11],[20].

Unfortunately, current for RESET of RRAM is larger than for flash memory as well as PCRAM and MRAM and, obviously, transistors with sufficient drive current are essential for device operation. Moreover, reading current cannot be lowered so much from the view point of the access time. Therefore an optimum range for RESET current should be around 100μA. Several papers report successful control of RESET current within this range [21], [22]. However, it has not been well understood what factors control RESET current.

Both 1T1R and 1D1R unit cell structures have been proposed for memory arrays. Clearly, considering RESET current a 1D1R architecture reduces area of unit memory cell area for a single purpose memory. In contrast, it seems that a 1T1R architecture is advantageous for application to embedded memory due to compatibility with CMOS processing and ease of circuit design.

4. Process Integration

RRAM can be fabricated as a part of conventional CMOS backend fabrication and, thus, from the view point of process technology, can be merely thought of as functional interconnection technology. Accordingly, a MLC or 3D integration of RRAM should inevitably surpass NAND in cost. In addition, characteristic resistance of RRAM can be controlled continuously, which satisfies the minimum requirement to achieve MLC [23]. However, for MLC, writing and access speeds of the device may have to be sacrificed, which reduces the fundamental advantage of RRAM. On the other hand, 3D integration is producible as an integral part of a multilayer interconnect scheme. Moreover, melting points of the metallic oxide films used for RRAM are higher than those of chalcogenide materials used for PCRAM. Therefore, compared with PCRAM it seems that RRAM should be robust with regard to any thermal budget required for 3D integration. An ultra high density memory consisting of stacked 1D1R structures corresponding to 3D integration is illustrated conceptually in Fig.1.

5 Reliability

Previous papers have discussed reliability characteristics of unit RRAM memory and indicate that it should have endurance of at least 100K rewrite cycles and good data retention at high temperature [4], [17]. Of course, further understanding of the physical cause of degradation and statistical evaluation are essential for an accurate reliability evaluation.

6. Conclusion

In this work, it has been possible to explain RRAM operation and, consequently, to control device operation. To proceed further, it is necessary to accumulate process integration experience, to secure statistically significant reliability data, and to turn the present development effort toward creation of the optimized circuit designs.

Table 1 Resistance switching materials

<table>
<thead>
<tr>
<th>Oxide</th>
<th>Electrode</th>
<th>Switching mode</th>
<th>SET</th>
<th>RESET</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>POMD</td>
<td>Ag, Pt</td>
<td>bipolar</td>
<td>&lt;10ns</td>
<td>&lt;100ns</td>
<td>[1],[3]</td>
</tr>
<tr>
<td>POMD</td>
<td>Pt</td>
<td>unipolar</td>
<td>10ns</td>
<td>5ns</td>
<td>[3]</td>
</tr>
<tr>
<td>STO SZO</td>
<td>Au</td>
<td>bipolar</td>
<td>100ns</td>
<td>100ns</td>
<td>[2]</td>
</tr>
<tr>
<td>NiO</td>
<td>Pt</td>
<td>unipolar</td>
<td>10ns</td>
<td>5ns</td>
<td>[21],[18]</td>
</tr>
<tr>
<td>TiOx</td>
<td>Pt</td>
<td>bipolar</td>
<td>&lt;30ns</td>
<td>&lt;30ns</td>
<td>[11],[20],[22]</td>
</tr>
<tr>
<td>CuOx</td>
<td>Ti</td>
<td>bipolar</td>
<td>&lt;100ns</td>
<td>&lt;100ns</td>
<td>[17],[21]</td>
</tr>
<tr>
<td>CuOx</td>
<td>Ni</td>
<td>unipolar</td>
<td>300ns</td>
<td>300ns</td>
<td>[17]</td>
</tr>
<tr>
<td>TiOx</td>
<td>Pt, TiN</td>
<td>unipolar</td>
<td>&lt;50ns</td>
<td>&lt;50ns</td>
<td>[16]</td>
</tr>
</tbody>
</table>

Fig.1 Final array structure for high density RRAM

References

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[18] K. Kinoshita, NVM workshop 2006, 84
[20] Y. Hosoi et al., Tech. Dig. of 2006 IEDM, 793
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