

J-7-1 Ru/TiO₂/ZrO₂/TiN (RIT-TiO₂/ZrO₂) Capacitor Structure for the 50nm DRAM Device and beyond

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Introduction

As the innovative scale-down of DRAM device continues, 50nm generation becomes close at hand. As shown in Fig. 1, to satisfy the cell capacitance of 25fF with 1.7 μ m storage-node height in 50nm design rule, the equivalent oxide thickness (Tox_{eq}) of a dielectric material should be as low as 0.8nm. TiN/HfO₂/TiN (TIT) capacitor has been successfully developed for 70nm generation [1], but it seems to be difficult to meet the requirements for sub-60nm device. When Ta₂O₅ or TiO₂ was implemented as the dielectric of the TIT capacitor to reduce Tox_{eq}, below 1.2nm, it was difficult to suppress the leakage current because of low barrier height and poor interface between TiN and high-k dielectric (Figure 2). On the other hand, Ru/Insulator/Ru (RIR) capacitor using high-k dielectrics has some problems yet to be solved, such as the contact-plug oxidation and Ru electrode agglomeration during the back-end process. In the previous study [2], we have proposed Ru(top)/Insulator/TiN(bottom) capacitor as an alternative for the DRAM capacitor below 50nm generation. The leakage currents of Ta₂O₅ and TiO₂ could be reduced by the application of Ru top electrode. And also a reliable storage-node was obtained with solid TiN bottom electrode. RIT-Ta₂O₅/HfO₂ was successfully developed corresponding to Tox_{eq} 1.1nm with 1fA/cell leakage current after full integration.

In this study, to reduce Tox_{eq} value lower than 0.8nm, we have introduced ZrO₂ as dielectric layers. We have compared and discussed the electrical characteristics of RIT-TiO₂/ZrO₂ and RIT-TiO₂/HfO₂ capacitors. The electrical properties after back-end metal-line integration and time-dependent-dielectric-breakdown behavior were also investigated.

Electrical behaviors of RIT capacitor

Table 1 shows the deposition methods and the precursors for the fabrication of RIT capacitors. TiN and Ru electrodes were deposited with CVD method and dielectric layers such as TiO₂, ZrO₂, and HfO₂ with ALD method, respectively. For ZrO₂, post annealing (Rapid thermal oxidation) was done to crystallize ZrO₂ layer.

Figure 3 shows the Tox_{eq} versus leakage current trend and the typical leakage current curves of RIT-TiO₂/ZrO₂ and RIT-TiO₂/HfO₂ capacitor, respectively. Although we could obtain low Tox_{eq} of 0.85nm with RIT-TiO₂/HfO₂ capacitor, the Tox_{eq} value was further reduced to 0.72nm with better leakage current for RIT-TiO₂/ZrO₂ capacitor. The Tox_{eq} is the value applicable enough to the 50nm device. Figure 4 shows TEM images of the RIT capacitors fabricated in the cylinder type structure. Double dielectric layers were uniformly deposited with good step coverage. On the other hand, very thin interfacial layers, especially in RIT-TiO₂/ZrO₂ capacitor, were found between the TiN electrode and the dielectric layer. In RIT capacitor, one of the critical issues was how to prevent the TiN bottom electrode from oxidation, because the dielectric layer as well as Ru top electrode were deposited in oxidation atmosphere. When the TiN bottom electrode was oxidized, both

Tox_{eq} and the leakage current increased due to the formation of the interfacial layer between TiN and the dielectric layer.

Figure 5 shows the leakage current curves with and without TiN electrode treatment. Rapid thermal oxidation (RTO) was done to suppress TiN oxidation. As shown in Figure 5, RTO-annealed RIT capacitor showed improved leakage current characteristics. To analyze the reason why the RTO treatment before the formation of the dielectric layer improved the electrical properties, TiN surface was analyzed by X-ray photoelectron spectroscopy (XPS). As shown in Figure 6, after the RTO treatment, N 1s XPS spectrum was broadened and clearly separated into two discrete spectral components. These two curves in the spectrum could be assigned to Ti-N bond and Ti-O-N bond, respectively. The Ti-O-N layer was considered to act as an oxidation barrier layer and was supposed to be major contribution in the improvement of the capacitor leakage current.

Integration of RIT capacitor

RIT-TiO₂/ZrO₂ and RIT-TiO₂/HfO₂ capacitors have been developed with cylinder-type capacitor in 512Mbits 90nm-DRAM device. Figure 7 shows the cross-sectional SEM image after metal-line integration. RIT-TiO₂/ZrO₂ and RIT-TiO₂/HfO₂ capacitors were successfully fabricated after metal-line integration without any defects. However, as shown in Figure 8, the leakage current of RIT capacitors was degraded after metal-line integration. Figure 9 shows the leakage current curves of the RIT capacitor according to the back-end process temperature. In the case of the back-end process temperature was maintained below 400°C, no degradation of leakage current was found.

Figure 10 shows the distribution of cell capacitance and leakage current. Superior cell capacitance about 50fF/cell was obtained with 2~3fA/cell leakage current at 0.9V with fairly good distribution. The time-dependent-dielectric-breakdown behaviors, as shown in Figure 11, also indicates that the RIT capacitor is reliable enough for the long lifetime.

Conclusions

RIT capacitors with TiO₂/ZrO₂ and TiO₂/HfO₂ layers were successfully fabricated for DRAM application of 50nm generation and beyond. Superior Tox_{eq} of 0.72nm was obtained with the low leakage current, below 1fA/cell at 0.9V. The leakage current after full integration showed little degradation when the back-end process temperature maintained below 400°C. The RIT capacitor also showed reliable lifetime over 10 years within the DRAM operation voltage.

References

- [1] J. H. Choi. et al., IEDM2003, p661-664, 2003.
- [2] K. H. Lee. et al., IEDM2004, p841-844, 2004.

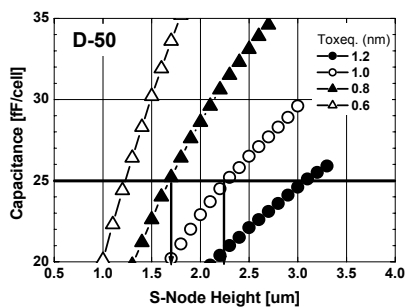


Fig. 1. Relationship between cell capacitance and node height.

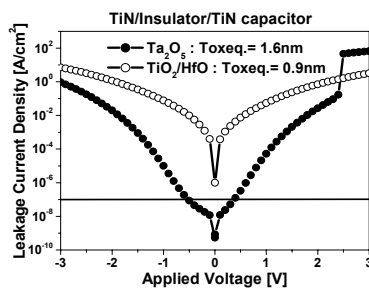


Fig. 2. Leakage current characteristics of TIT capacitor with high-k dielectric materials.

Table. 1. Deposition methods and precursors for the fabrication of RIT capacitor.

Storage Node	CVD TiN TiCl ₄ + NH ₃
Dielectric Deposition	ALD HfO ₂ Hf(NetMe) ₄ + O ₃
	ALD ZrO ₂ Zr(NetMe) ₄ + O ₃
	ALD TiO ₂ Ti(OiPr) ₄ + O ₃
Top Electrode	CVD Ru Ru(EtCp) ₂ + O ₂

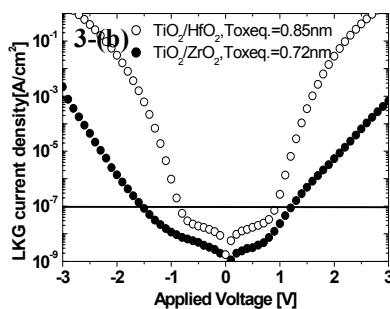
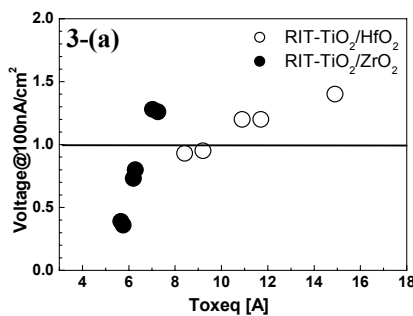


Fig. 3. Leakage current characteristics of RIT capacitors.
(a) Toxeq. vs. leakage current trend. (b) Leakage current curves.

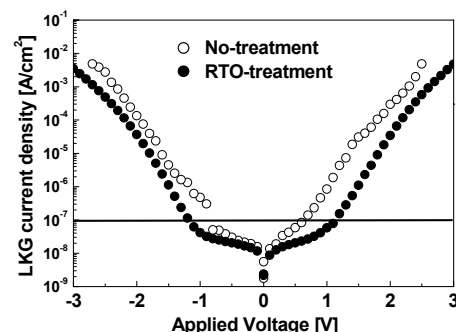


Fig. 5. Leakage current curves of RIT-TiO₂/HfO₂ capacitors.

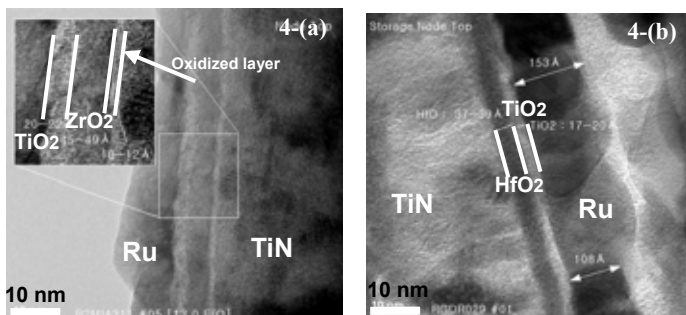


Fig. 4. TEM images of RIT capacitor.
(a) TiO₂/ZrO₂ capacitor (b) TiO₂/HfO₂ capacitor.

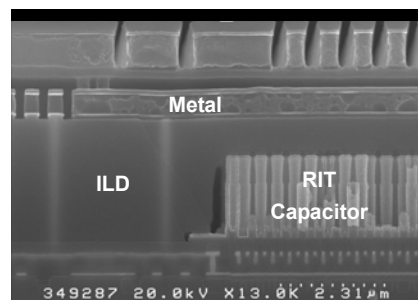


Fig. 7. SEM image of fully integrated RIT capacitor.

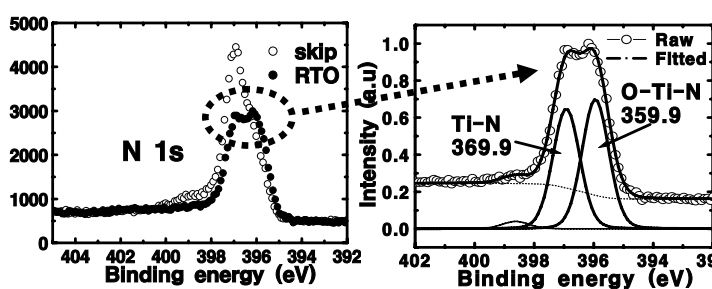


Fig. 6. XPS results of TiN surfaces with or without RTO treatment.

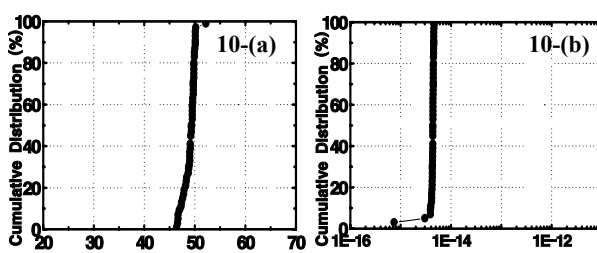


Fig. 10. Distribution of cell cap. and leakage current density of RIT TiO₂/ZrO₂ capacitor. (a) cell capacitance and (b) leakage current.

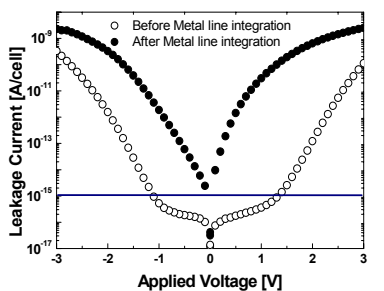


Fig. 8. Leakage current curves before/after metal-line integration.

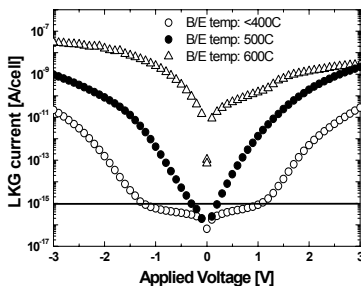


Fig. 9. Leakage current curves according to the backend-process temperature.

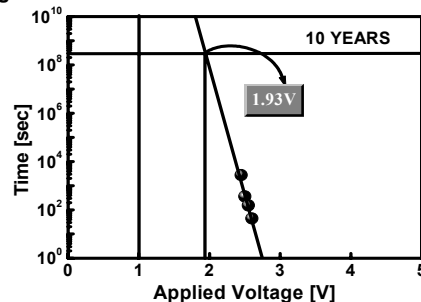


Fig. 11. Time-dependent-dielectric-breakdown (TDDB) behavior of RIT-TiO₂/ZrO₂ bilayer.