Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 1152-1153

J-7-4

Effect of Boron-Nitride Formation at the Interface of Diffusion Barrier in Tungsten Polymetal Gate Stacks on Gate Interfacial Resistance

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Abstract

We investigated the effect of boron at the interface of diffusion barrier in tungsten poly gate stacks on gate contact resistance (Rc) between tungsten and p+ poly-Si in memory devices. By preventing B-N formation at the bottom of WN for Ti/WN barrier, gate Rc could be reduced effectively compared to WSix/WN barrier.

1. Introduction

Tungsten polymetal gate electrode is an attractive candidate for high speed dynamic random access memory (DRAM) devices in a narrow gate length less than 100nm, due to a lower sheet resistance (Rs) than that of conventional tungsten polycide gate stacks. However, an appropriate choice on diffusion barrier should be made to ensure low gate Rc. Recently, in gate electrode process, thermally stable WSix/WN [1] and Ti/(TiN)/WN [2] barriers were proposed for the reduction of gate Rc. However, extensive study relating the effect of barrier metals on p+ gate Rc has not been made. In this article, we investigated the effect of diffusion barrier on the gate Rc in tungsten dual poly gate stacks. Proposed gate Rc model will be verified using physical and electrical characterization.

2. Experimental

After the pre-cleaning of p+ poly-Si surface, various barrier metals such as Ti, TiN, WN, WSix and amorphous Si (a-Si) were deposited by sputtering or chemical vapor deposition (CVD) method. TiN and WN layer was deposited by reactive sputtering method in the gas mixture consisting of Ar and N_2. Tungsten films with a thickness of 40nm were deposited on the deposited barrier metals. Each gate stack was examined by cross-sectional high-resolution transmission electron microscopy (HRTEM). For the material characterization, boron profiles were probed by secondary ion mass spectroscopy (SIMS). For the investigation of composition and the chemical binding state of interfacial layer, X-ray photoelectron spectroscopy (XPS) was conducted with non pattern wafers, after stripping top tungsten layer using H_2O_2 chemical. Gate Rc was measured by fabricating four-terminal Kelvin circuits. To see signal delay effect induced by the interfacial resistance on transistor devices, ring oscillator (R/O) structures were fabricated and measured.

3. Result and Discussion

A. B-N resistance model

Figure. 1 describes the cross-sectional HRTEM images of the gate stacks (WSix/WN and Ti/WN barrier). In the case of p+ poly gate stack, dissociated nitrogen from the WN layer, during post thermal process, could easily interact with out-diffused boron, creating insulative B-N compound inter-layer which could lead to the increase of gate Rc. B-N peak measured from XPS is clearly observed for WSix/WN barrier, as shown in Fig. 2. It is considered that boron has reached denuded WN through WSi_2 during post annealing. Measured gate Rc between p+ poly-Si and tungsten electrode for each gate stacks is shown in Fig. 3. Huge increase of gate Rc was observed for the case of WSix/WN barrier compared to Ti/WN barrier. The amount of B-N in Ti/WN barrier seems to much smaller than that of WSix/WN barrier. Accordingly, we can model (So called B-N resistance model) that the created B-N inter-layer at the gate interface should lead to increased gate Rc.

B. Ti(N) inserted barrier

Three different gate barrier metals (Ti(3nm), TiN(4nm) and Ti(3nm)/TiN(4nm)) were inserted between p+ poly-Si and WN(5nm), as shown in Fig. 4. In the Ti/WN barrier, stable TiN-TiB_2-BN ternary phase can exist at the interface [3]. Much portion of out-diffused nitrogen from WN reacts with Ti layer, which leads to TiN formation. Most volume of the Ti layer was converted into TiN layer during annealing. Created TiB_2 compound at the grain boundary of $TiSi_2$ layer could cause drastic limitation of boron out-diffusion into the WN [4]. Therefore, relatively small portion of nitrogen could be contributed to the B-N formation. In the case of Ti/TiN/WN barrier, the inserted TiN does not interact with dissociated nitrogen during post thermal treatment, due to its thermally stable characteristic. The difference of TiN thickness between Ti/WN and Ti/TiN/WN after annealing is less than 1nm. So we could neglect the effect of TiN layer which could behave as an additional diffusion barrier against boron. Therefore, larger amount of nitrogen could contribute to the B-N reaction than Ti/WN barrier, leading to larger amount of B-N layer, which resulted in increased gate Rc. In the case of TiN/WN barrier, additional inter-layer could be formed besides the formation of B-N. Si-N dielectric inter-layer could be created by the reaction between nitrogen ambient and poly-Si during the reactive sputtering process of TiN. Interfacial chemical states for Si-N dielectric were analyzed by conducting XPS measurement after removal of top tungsten electrode. Fig. 5 shows that only TiN/WN barrier exhibits Si-N dielectric peak in Si 2p spectrum. With double stacked diffusion barriers (TiN/Si-N) which could prevent out-diffusion of boron, the amount of B-N layer should be the smallest among the examined gate stacks. However, the existence of dielectric Si-N layer could lead to huge increase of gate Rc. Fig. 6 shows measured SIMS depth profiles of boron in p+ poly-Si. We can quantify the created B-N layer indirectly by measuring boron concentration where B-N reaction could occur. Ti/TiN/WN barrier shows the highest remaining boron concentration at B-N reaction region and TiN/WN barrier exhibits smallest amount among the gate stacks. Fig. 7 shows electrically measured Kelvin gate Rc, which is a consistent result with B-N resistance model.

C. WSix inserted barrier

Three different gate barrier metals (WSix(10nm),WSix(20nm) and a-Si(8nm)/WSix(10nm)) were inserted, as shown in Fig. 8. In spite of the thickness increase of the WSix, the difference of the created B-N layer should be small due to the high segregation coefficient of boron to WSix. Fig. 9 shows SIMS depth profiles of boron in poly-Si. a-Si/WSix/WN barrier shows much reduced boron concentration at B-N reaction region due to the existence of a-Si acting diffusion buffer against boron. Addition of Si-grains caused by the a-Si insertion in place of WSi_2 grains breaks the diffusion path of boron [5]. Fig. 10 shows R/O delay characteristics. WSix(20nm)/WN and WSix(10nm)/WN barrier shows similar R/O delay characteristics at an identical propagation delay time (Tpd). a-Si/WSix/WN barrier shows smaller R/O delay than those of WSix/WN barriers, which is a consistent result with SIMS analysis. Ti/WN barrier shows much smaller value of R/O delay than those of WSix inserted barriers, which is the same trend of gate Rc, as shown in Fig. 3.

4. Conclusion

We studied the effect of B-N formation at the interface of diffusion barrier in tungsten poly gate stacks on the gate Rc. Based on our B-N resistance model, we varied gate diffusion barrier to see the effect of formed B-N inter-layer for WSix and Ti(N) inserted barrier metal. The measured boron concentration at the region where B-N reaction could explain the difference of electrically measured data. Ti/WN barrier is found to be a best choice for reducing p+ gate Rc value in tungsten dual poly gate process, which could satisfy the high speed requirement of future DRAM devices.

References

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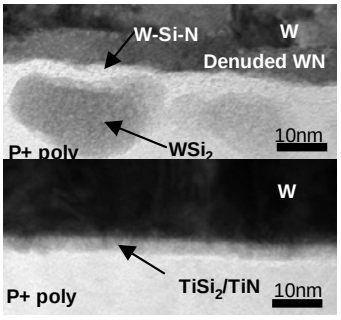

Fig. 1. Cross sectional HRTEM images : (Top) WSix/WN barrier, (Bottom) Ti/WN barrier.

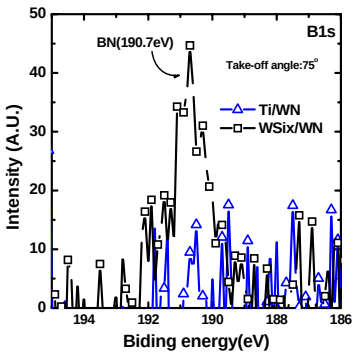

Fig. 2. The measured B 1s XPS spectra. WSix/WN barrier shows BN peak.

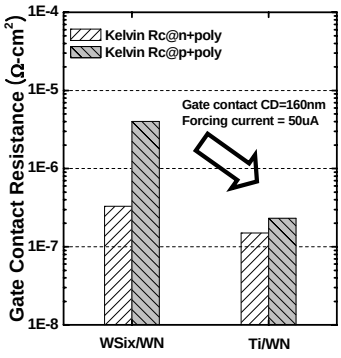

Fig. 3. Gate Rc measured by 4-thermial Kelvin method. Ti/WN barrier shows much smaller value than that of WSix/WN barrier in PMOS.

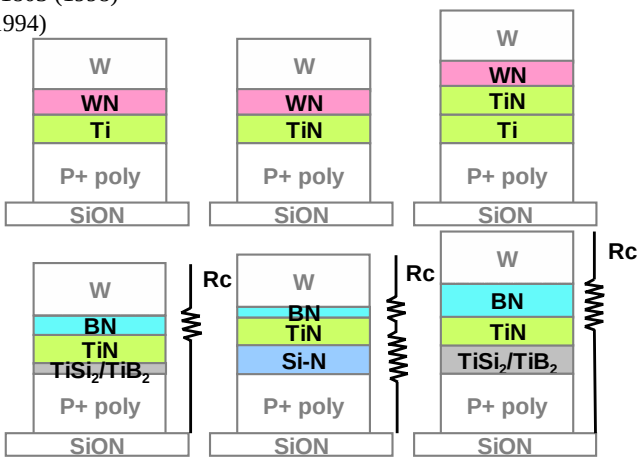

Fig. 4. Cross sectional schematic diagram of gate stacks with different kinds of Ti(N) inserted barrier: (Top) as deposited, (Bottom) after post annealing, Resistance symbol for each gate stack shows the created parasitic gate Rc.

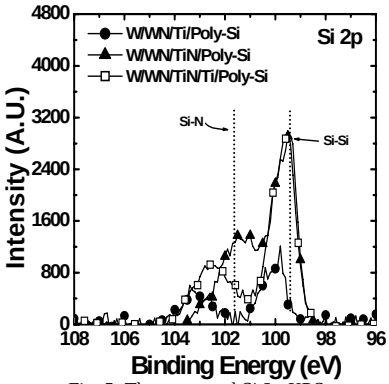

Fig. 5. The measured Si 2p XPS spectra for gate stacks. TiN/WN barrier shows Si-N dielectric peak.

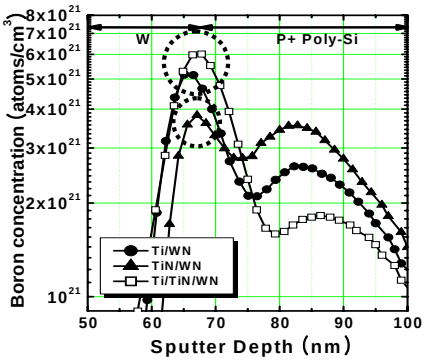

Fig. 6. Boron SIMS depth profile for Ti(N) inserted gate stacks. Denoted dotted circle indicates the position where the B-N reaction could happen.

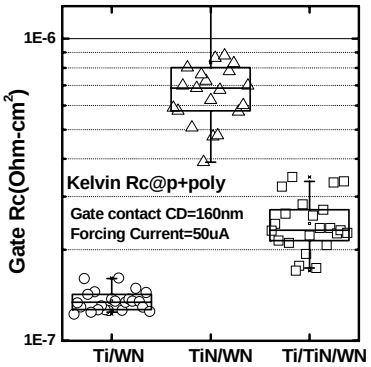

Fig. 7. The measured Kelvin gate contact resistance. Ti/WN barrier shows the lowest value.

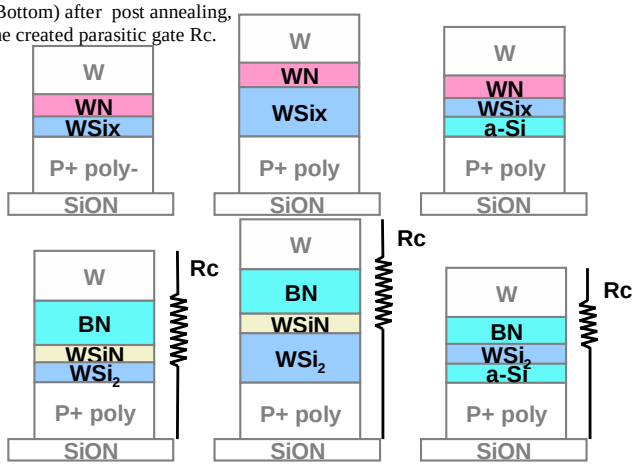

Fig. 8. Cross sectional schematic diagram of gate stacks with different kinds of WSix inserted barrier: (Top) as deposited, (Bottom) after post annealing. Resistance symbol for each gate stacks shows the created parasitic gate Rc.

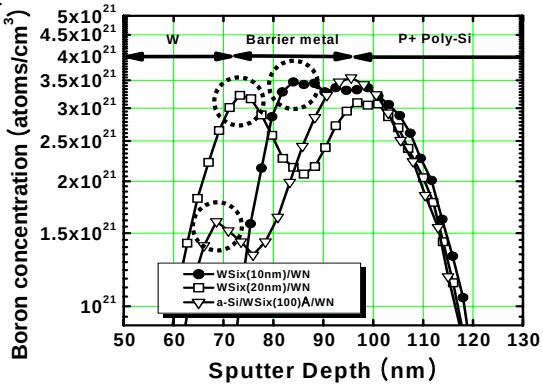

Fig. 9. Boron SIMS depth profile for WSix inserted gate stacks. Denoted dotted circle indicates the position where the B-N reaction could happen.

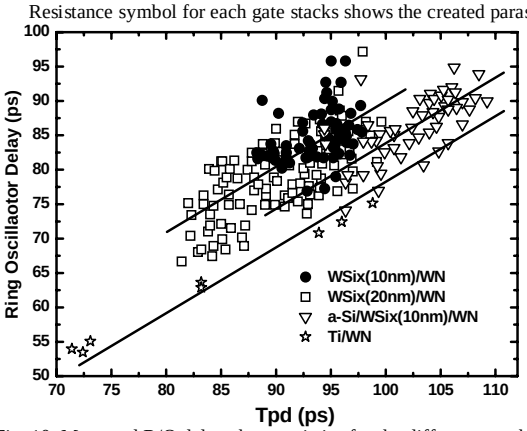

Fig. 10. Measured R/O delay characteristics for the different gate barrier metals. R/O delays are plotted at the corresponding propagation delay time (Tpd). Extrapolated lines for measured data are drawn for each barrier.