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Digital Circuits with Carbon Nanotube Transistors

Arijit Raychowdhury[+]*, Juanita Kurtin[+], Kaushik Roy*, Vivek De[+], Ali Keshavarzi[+]
[+]Intel Corporation and *Purdue University

Abstract: In this paper we investigate carbon nanotube field effect transistors (CNFETs) for high performance logic circuit applications.

1. Introduction

Carbon nanotube field effect transistors (CNFETs) are being extensively researched both in industry and in academia as possible high mobility channel material with very good carrier transport properties [1-5]. In this paper we will focus on the requirements for using CNT transistor arrays as switches in circuits. For details of various aspects of digital circuits utilizing Schottky barrier CNFETs (SB CNFETs) for high performance logic applications the readers are directed to [1-3]. Although CNFETs operating as MOSFETs are desirable, most of the experimental devices are SB in nature where the gate modulates a tunneling barrier at the source-channel junction (Fig. 1). Transistors based on CNTs have demonstrated that they meet the basic and minimum requirements that a useful device should have gain, signal to noise ratio and scalability.

2. Circuits Challenges and Limitations

In this section we will discuss how DC and AC circuit operations are impacted by the properties and geometry of the CNTFETs [1-2]. We studied noise margin (NM) and voltage swing (VS) that are critical in inverter voltage transfer characteristics (VTC) for circuits. Our analysis showed in Fig. 2 that NM and VS of circuits utilizing SB CNFETs are sensitive to the choice of supply voltage and CNT diameter (bandgap). If we had to pick a point from this data, we would have selected supply voltage of 0.5V and diameter of ~ 1 nm from NM and VS point of view. The fact that we need small diameters and low supply voltage is interesting as Si-based MOSFET's NM and VS do not have this much supply voltage dependency and are not limited by process window.

AC and transient operations are also impacted with our choice of CNT transistor, diameter and supply voltage. Our data regarding performance versus power trade-off of a FO4 RO shows how the choice of our transistor impacts this trade-off (Figs. 3&4). The transistor I-Vs play a major role in Fig. 4 results. It is reasonable that small diameter (0.8 nm) tube SB CNFETs have produced performance versus power curve that corresponds to low performance and low power. What is interesting is that performance vs. power tradeoff for large diameter transistors (2 nm) show that these ROs have low performance for high power. The reason for this behavior is the large leakage in large diameter tubes, which results in low Ion/Ioff ratio and slow switching. Thus larger diameter SB CNFETs have no advantage in terms of delay and are undesired in complementary CMOS. Optimum performance requires D of ~ 1.5 nm and low supply voltage.

3. Transistor Arrays for Realistic Circuits

In order to have fan-out, drive fixed large loads such as interconnect in circuits and to have drive currents compatible with silicon technology, we need to use multiple CNTs in the channel of the transistor and effectively pack as many of them as we can.

Fig. 5 shows the normalized delay as a function of inter-tube spacing for different capacitive loads [2]. This figure shows that no mater what load capacitance is used, the tubes need to be packed relatively densely in order of 1 to 5 diameters apart. This is a very challenging task for fabrication if we consider that the diameter of the CNTs of interest is around 1 nm and hence the spacing should be below 5 nm. Fig. 6 analyzes the minimum array packing density requirements by studying Ion per footprint as a function of spacing between the CNT tubes. We have considered two scenarios: (1) a simulated scaled high performance CNFET with a nominal "on" current per tube of 50uA, and (2) an experimentally achieved value of ~ 20uA [4]. Assuming current per footprint of 1 mA/um for Si, our data suggests that CNTs should be packed denser than 50 nm apart to be better than Si (20 nm apart for best experimentally reported CNFETs).

The most important observation is that CNT transistor array practically cannot tolerate any metallic tubes. We need 99.95% pure semiconducting tubes to achieve Ion/Ioff ratio of 1000 and if we use a natural mix of 33% metallic tube in CVD-grown CNTs in the array, then Ion/Ioff ratio degrades to less < 2 (Fig. 8). This is critical because no matter how variation tolerant is our structure, device and our circuits, from digital applications point of view, we need to purify the semiconducting tubes to better than 99.95% for Ion to Ioff ratio.

4. Summary and Future Challenges

In this paper we discussed the potential of carbon nanotube based FETs in future high performance circuits and mentioned key targets that devices need to achieve for digital circuits. However critical challenges, like, removing metallic tubes, tube packing density in arrays, doping, self-aligned devices, parasitic control and device structure optimization, fabrication of nano contacts and dealing with high power densities remain. In spite of these challenging barriers, research continues on CNTs because CNFETs may deliver high performance characteristics and scalability for the future.

References

[1] A. Raychowdhury, et. al., IEEE TED, Nov. 2006, pp. 2711-2717.
[2] A. Keshavarzi, et. al., IEEE TED, Nov. 2006, pp. 2718-2726.
[3] A. Keshavarzi, et. al., 2006 A-SSCC, pp. 415-418.
[4] A. Javey et. al., Nature, Vol. 427, 2003, pp. 654-657.
[5] Z. Chen, et. al., 2007 ISSCC, pp. 68-69.

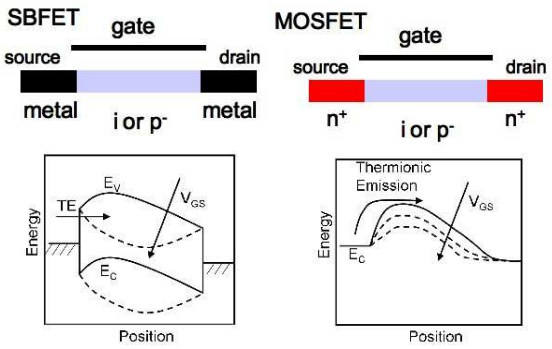


Fig. 1: Schematics showing Schottky Barrier and MOS CNFETs and their principle of operation

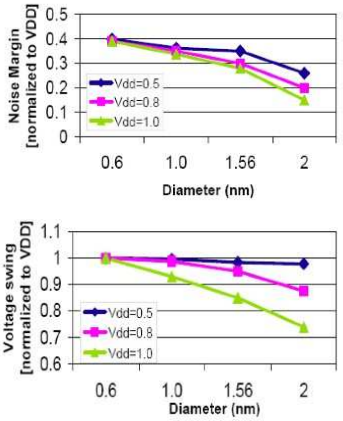


Fig. 2: Noise Margin and voltage swing as a function of nanotube diameter for different supply voltages

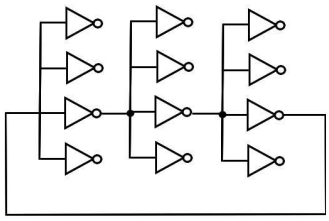


Fig. 3: Schematic of a FO4 Ring Oscillator (RO)

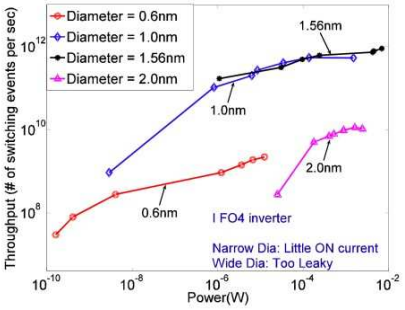


Fig. 4: Performance-power tradeoff in SB based FO4 inverter for different nanotube diameters

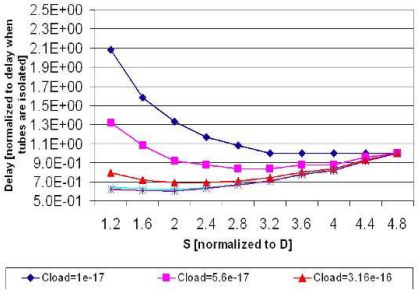
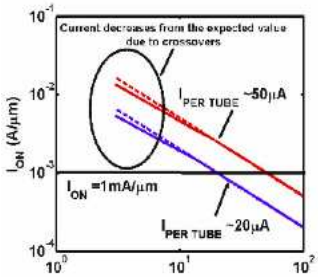


Fig. 5: Normalized delay as a function of nanotube spacing for different load conditions.



Spacing (nm)	ON Current per footprint (mA/um)		Comment
	$I_{PER\ TUBE\ \sim 50uA}$	$I_{PER\ TUBE\ \sim 20uA}$	
100	0.523	0.2	Spacing experimentally feasible today
54	1	-	Density to meet Si MOSFETs
20	-	1	
3	17	7	High performance Array

Fig. 6: ON current in a CNFET array as a function of tube density

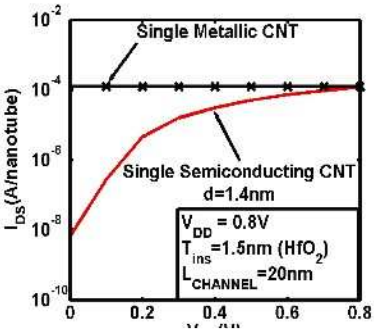
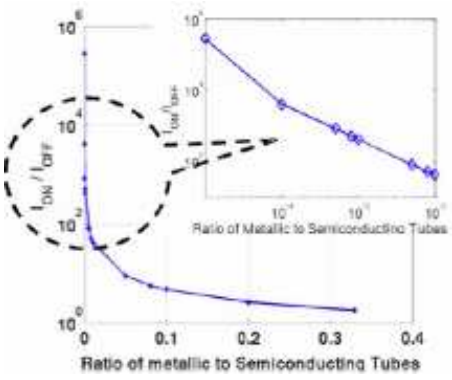


Fig. 7: I-V characteristics of a metallic and a semiconducting nanotube



% metallic	Ion/Ioff ratio	Comment
33	1.85 (~2X)	Natural mix of metallic and semiconducting tubes
10	4.75 (~5X)	PECVD CNT growth for improved semiconducting tube yield [Dai]
0.5	84 (~100X)	Aggressive Ion to Ioff target of 100X
0.05	831 (~1000X)	Good Ion/ Ioff ratio with 99.95% semiconducting tubes

Fig. 8: Role of metallic tubes in the Ion/Ioff ratio in CNFET arrays