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Single charge sensitivity of single-walled carbon nanotube single-hole transistor

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1. Introduction

We succeeded in observing the single charge transition near the channel of single-walled carbon nanotube (SWNT) single-hole transistor (SHT).

Abrupt discrete switching of the source-drain current is observed in the electrical measurements of SWNT SHT. These random telegraph signals (RTS) are attributed to charge fluctuating charge traps near the SWNT SHT conduction channels. Evolution of the current-switching behavior associated with the occupancy of individual electron traps is demonstrated and analyzed statistically.

2. Experimental

The sample was prepared as follows. A p-type silicon wafer with a thermally grown oxide of 300 nm is used as a substrate. The layered catalysts of Fe/ Mo/ Si (3/ 20/ 40 nm) were patterned on the substrate using the conventional photo-lithography process. The distance between two catalysts for the source and drain was 5 μm. SWNT is grown between two catalysts by chemical vapor deposition using mixed gas with ethanol, hydrogen and argon. Co electrodes were patterned by using electron-beam lithography process. The electrodes were deposited on the patterned catalysts for the source and drain and the back side of Si substrate for the gate. The distance between the source and drain was as short as 73 nm. Finally, silicon dioxide layer was deposited on the SWNT SHT. Thus, back gate type SWNT SHT was fabricated as shown in Fig. 1.

3. Results and discussions

In the drain current-gate voltage characteristics of SWNT SHT under the drain voltage of 11 mV at 7.3 K, drain current showed periodic peaks and valleys structure, which had two periods as shown in Fig.2 (a). The large period was attributed to Coulomb oscillation characteristic, the period of which was about 3 V. the small period was attributed to the quantum interference property of hole, the period of which was 0.5 V as shown in Fig 2 (b). The drain current was observed only in negative gate voltage region, which indicates that the measured SWNT SHT has the p type semiconductor property.

The SWNT SHT was covered by deposited silicon dioxide layer to prevent SWNT SHT from absorbing and releasing molecules because adsorption and desorption of molecules from SWNT SHT usually induced hysteresis characteristics in the drain current-gate voltage characteristics. Owing to the covering silicon dioxide layer, the SWNT SHT showed almost no hysteresis characteristics as shown in Fig. 3.

The SWNT SHT shows RTS as shown in Fig. 4 (a) and (b), which were attributed to charge fluctuating charge traps near the SWNT SHT conduction channels. The RTS appeared as two levels, upper level and lower level, of drain current, the occupation probabilities of which was depended on the applied gate voltage. We assumed the simple model as shown in Fig. 4 (c) to explain the gate voltage dependent occupation probabilities of RTS.

Figure 5 shows the gate voltage dependence of the ratio of the occupation probabilities of upper level and lower level. According to equilibrium statistical mechanics, this probability ratio is given by [1)]

$$P_{\mathrm{upper}}/P_{\mathrm{lower}} = (g_1/g_2)\, e^{-\beta(Ef-Et)}) = (g_1/g_2)e^{-\beta\Delta E} \qquad (1)$$

where g_1 is the degeneracy of the Fermi level, g_2 is the degeneracy of the trap state, E_f is the Fermi energy, and E_t is the trap state energy. (E_t includes contributions of the electrostatic potential induced by V_g, the intrinsic trap energy, and the Coulomb charging energy.) Assuming a linear dependence of ΔE on V_g, i.e., $\Delta E = ce(V_g - V_0)$, where c is gate modulation coefficient (the ratio of applied gate voltage and modulated potential energy) and V_0 is offset voltage, which are constants.

From Fig. 5 and Eq. (1), we could estimate the c and ΔE as c=0.016 and ΔE=3.2 meV. Additionally, using coaxial cylinder model, we could estimate the distance: L between the trap and the channel of SWNT SHT as L=1.03 nm.

We succeeded in observing the single charge transition near the channel of SWNT SHT at 7.3 K. The observed RTS was depended on the applied gate voltage. We estimated the distance between the trap and the channel of SWNT SHT as L=1.03 nm.

[1] H. B. Peng *et al.*, Appl. Phy. Lett., **89**, 243502 (2006)

[2] K. Matsumoto *et al.*, Jpn. J. Appl. Phys. **42**, 2415 (2003)

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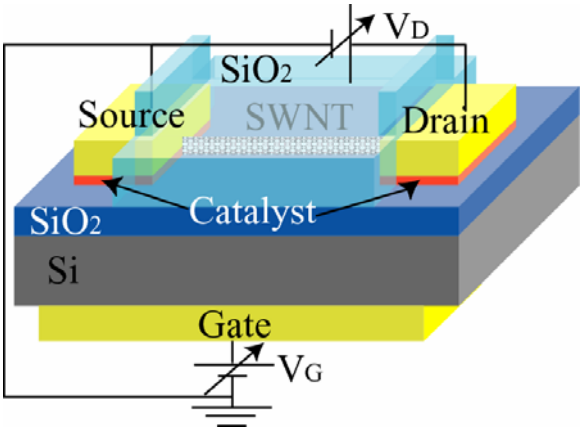

Figure 1. Schematic of SWNT SHT, which was covered by silicon dioxide layer. The channel length of which was 73 nm.

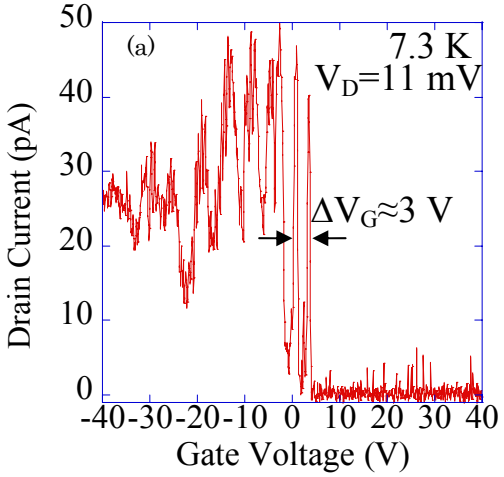

Figure 2 (a). Coulomb Oscillation Characteristic at 7.3 K

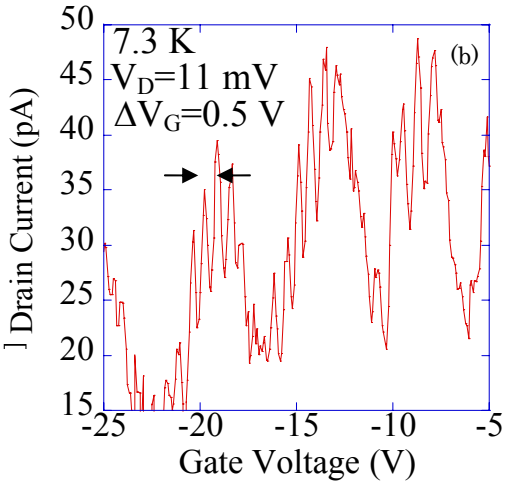

Figure 2 (b). The quantum interference property of hole

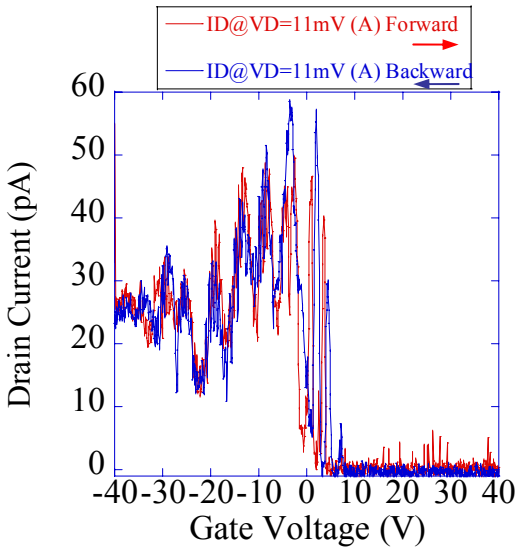

Figure 3. Gate voltage dependence of drain current characteristics, the gate voltage was applied from -40 V to -40 V via 40 V.

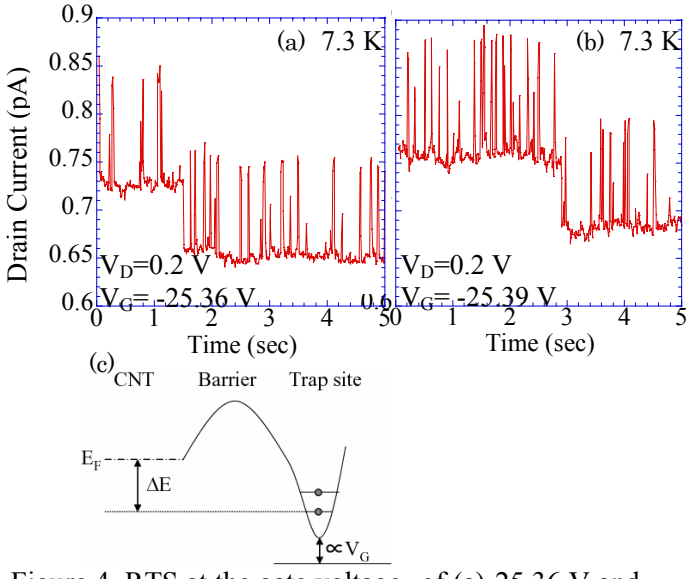

Figure 4. RTS at the gate voltage of (a)-25.36 V and (b) -25.39 V. (c) schematic model of charge traps

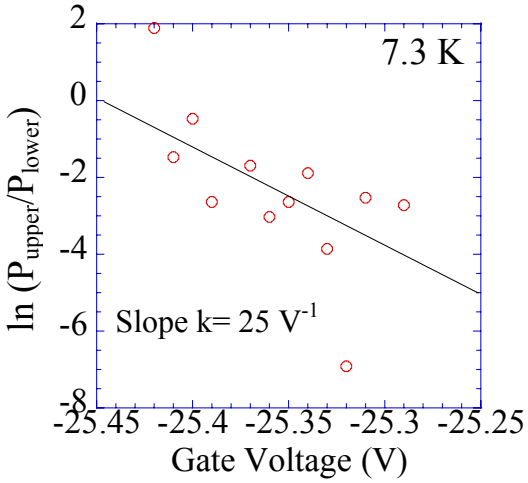

Figure 5. The gate voltage dependence of ratio of P_{upper} and P_{lower}