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Dual Metal Gate MOSFETs with Symmetrical Threshold Voltages Using Work Function Tuned Ta/Mo Bi-layer Metal Gates

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1. Introduction

Metal gate technology and new transistor structures such as a FD-SOI MOSFET and a multi-gate MOSFET have actively been investigated to meet the requirements of further device scaling. The work function of the metal gates for the FD-SOI and multi-gate MOSFETs is required to be 0.1-0.15 eV lower/higher than the midgap for n-/p-MOSFETs [1]. However, the process integration of the dual metal gates is still a challenging issue. Samavedam *et al*. reported on the integration process of TiN and TaSiN gates [2]. In their work, however, the gate dielectrics were exposed to a series of wet chemical processes for the etching-off of a TiN gate, which may degrade the integrity of the gate dielectrics. As an alternative technology without the metal etch-off process, it was reported that the interdiffusion of different metal stacks gave different work functions (WFs) for the n- and p-MOS gates [3,4]. We selected the combination of Mo with a high WF (4.95 eV) for the (110) plane [5] and Ta with a low WF (4.25 eV) [5] for the interdiffusion dual metal gate process [6] from the viewpoint of the superior thermal robustness. In this study, MOSFETs with a Mo gate and a Ta-on-Mo stacked gate were fabricated through the gate first process including S/D activation annealing. The device characteristics are presented in terms of the effective work function (EWF), the threshold voltage (V_{th}), and the carrier mobility.

2. MOS Capacitor Characterization

MOS capacitors with a single Mo layer and a Ta-on-Mo stack were fabricated. The Mo layers were deposited by a RF magnetron sputtering with an Ar pressure at 1.0 Pa, which was optimized to minimize the process damage. For the Ta/Mo stack gate, the underlying Mo thickness was set at 4 nm or 8 nm. Interdiffusion annealing (IDA) was carried out at 700^{o}C in a vacuum for both the Mo and Ta/Mo gates to enhance the diffusion of Ta into the underlying Mo layer. The cross sections of the capacitors with Mo and Ta/Mo(8 nm) gates after the IDA are shown in Fig.1. The continuous feature of the underlying Mo layer for the Ta/Mo gate is preserved even after the IDA. It is also shown that integrity of the metal/SiO_2 interfaces for both the samples is preserved.

The C-V curves of the Mo and Ta/Mo gate samples show the significant difference in the flat band voltage (Vfb) between the Mo and Ta/Mo gates (Fig.2). The Ta/Mo gates with Mo thickness of 4 nm and 8 nm represent almost identical C-V curves. Namely, the Mo thickness variation from 4 to 8 nm does not significanty influence on the Vfb. The EWFs of the Mo and Ta/Mo gates were estimated from the Vfb-EOT plots (Fig.3). The Ta/Mo gate exhibits a significantly decreased EWF (4.42 eV) in comparison with the single Mo gate (5.04 eV). Assuming a midgap level at 4.6 eV, the EWF for the Mo gate is 0.44 eV higher than the midgap and that for the Ta/Mo gate is 0.18 eV lower than the midgap (Fig.4). Namely, the Mo and Ta/Mo gates are suitable for the p-MOS and n-MOS gates and satisfy the FD-SOI and multi-gate MOSFETs requirements [1].

3. MOSFET Characterization

To certify the EWF tuning using the Mo and Ta/Mo gates in the transistor performance, the Mo and Ta/Mo-gated MOSFETs were fabricated through the processes shown in Fig.5. For the Ta/Mo stack gate, the underlying Mo thickness was set at 8 nm and the 30-nm-thick Ta was subsequently deposited. The 12-nm-thick Mo was additionally deposited on the Ta/Mo stack to obtain the better electrical contact to the Al metallization. Gate electrode patterning was successfully carried out by RIE using a CHF_3/O_2 plasma for the Mo and a SF_6/O_2 plasma for the Ta (Fig.6). Then, the self-aligned ion implantation into the S/D, the IDA, and the rapid thermal annealing (RTA) for the S/D activation were carried out.

Figure 7 shows the Id-Vg characteristics of the Mo and Ta/Mo gated MOSFETs. The V_{th} for the Mo and Ta/Mo gated n-MOSFET are estimated to be 0.89 V and 0.53 V, respectively. Namely, the Ta/Mo interdiffusion causes a 0.36 V decrease in the V_{th}. On the other hand, the V_{th} for the Mo gated p-MOSFET is estimated at -0.45 V. Thus, the Ta/Mo gated n-MOSFET and the Mo gated p-MOSFET represent almost symmetrical Id-Vg characteristics and are suitable for the CMOS operation.

The electron mobility for the Mo and Ta/Mo gates and the hole mobility for the Mo gates were evaluated using a standard split C-V technique at 10 kHz [7] (Fig. 8). The Ta/Mo gated n-MOSFET exhibits higher electron mobility than that of the Mo gated n-MOSFET. This means that the EWF tuning by the Ta/Mo bi-layer gate does not cause mobility degradation. On the contrary, another approach to reduce the Mo EWF by using nitrogen ion implantation was reported to cause mobility degradation due to the implantation damage [8]. Thus, the Ta/Mo bi-layer technique has an advantage for the EWF tuning. It is noteworthy that the hole mobility of the Mo gated p-MOSFET keeps the high value and the deviation from the universal curve is smaller than that for the electron mobility of the Mo gated n-MOSFET.

4. Summary

The Ta/Mo stack gate provides a significantly lower EWF (4.42 eV) than the single Mo gate (5.04 eV) without any etching-off process of the gate metals. The n-/p-MOSFETs with Mo and Ta/Mo gates were successfully fabricated through the gate first process and provided almost symmetric V_{th} (0.53/-0.45 V). The Ta/Mo stack gate does not cause degradation in the electron mobility compared with the single Mo gate. We conclude that the Mo and Ta/Mo gates can be suitably used as the dual work function metal gates of FD-SOI and multi-gate MOSFETs.

References

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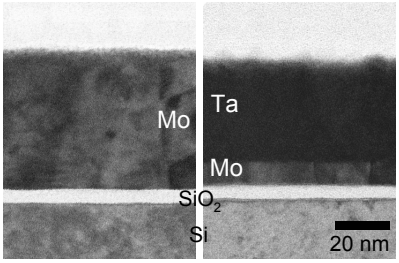

Fig.1 Cross sections of MOS capacitors with Mo(50 nm) and Ta(40 nm)/Mo(8 nm) gates obtained by scanning TEM.

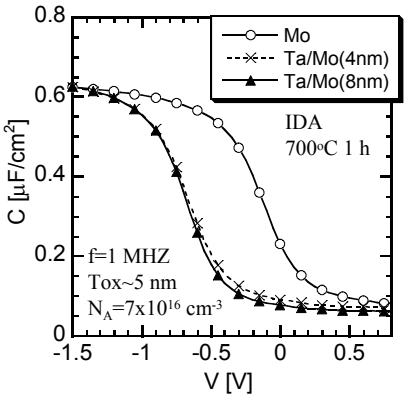

Fig.2 C-V curves for Mo, Ta/Mo(4 nm), and Ta/Mo(8 nm) gates. Stacking Ta on Mo causes significant Vfb difference. The Ta/Mo gates with 4 and 8 nm-thick-Mo provide almost identical C-V curve.

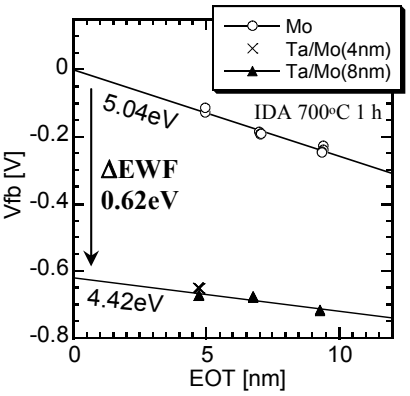

Fig.3 Vfb-EOT plots to evaluate EWF of Mo and Ta/Mo gates. Significant EWF difference (0.62 eV) between the Mo and Ta/Mo(8 nm) gates is obtained. The plots for the Ta/Mo(4 nm) gate almost coincide with those for the Ta/Mo(8 nm) gate.

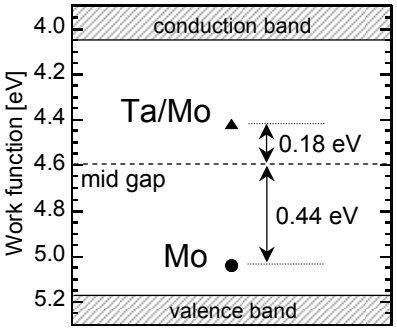

Fig.4 The EWFs of Mo and Ta/Mo gates compared with conduction band and valence band levels of Si.

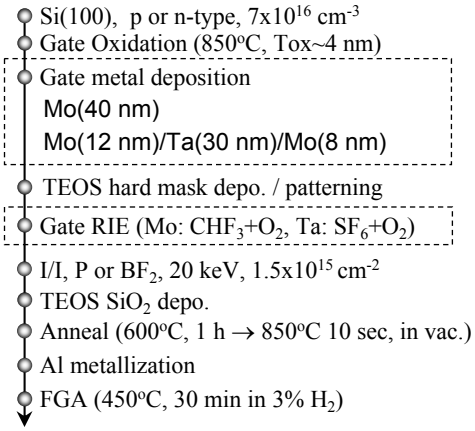

Fig.5 Process flow for Mo and Ta/Mo gated MOSFETs.

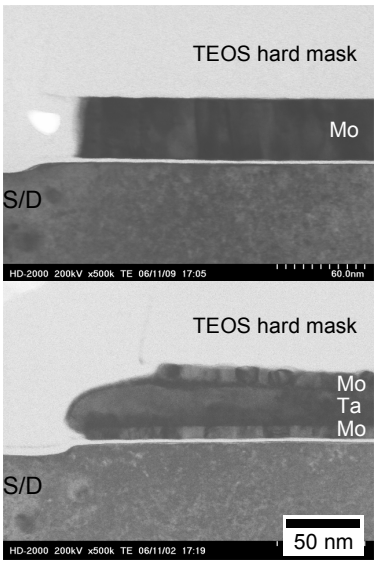

Fig.6 Gate edge profiles for Mo and Mo/Ta/Mo gates. Influence of gate over-etching is negligible.

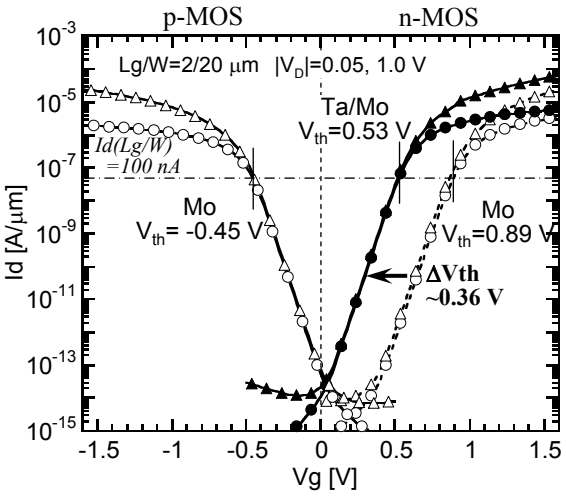

Fig. 7 Id-Vg characteristics of Mo and Ta/Mo gated n-MOSFETs and Mo gated p-MOSFET. The Ta/Mo gated n-MOSFET and the Mo gated p-MOSFET exhibit almost symmetrical characteristics.

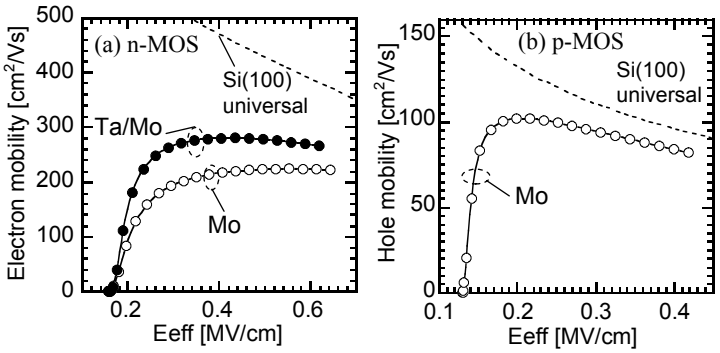

Fig. 8 (a) Effective electron mobility for Mo and Ta/Mo gated n-MOSFETs and (b) effective hole mobility for Mo gated p-MOSFET. The universal mobility curves of SiO_2/Si(100) [7] are shown as reference.