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TiN Gate Work Function Control Using Nitrogen Gas Flow Ratio and RTA-Temperature

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1. Introduction

Metal gate work function control is the most important issue to set a correct threshold voltage (V_{th}) for lightly doped channel MOSFETs such as FinFETs. In the past few years, as one of the promising metal gate materials, the sputtered titanium nitride (TiN) has widely been studied for planar CMOS devices [1-3] and non-planar FinFETs [4, 5] due to its high purity. However, there have been no systematical studies regarding the sputtered TiN gate work function (ϕ_{TiN}) control by using nitrogen gas flow ratio ($R_N = N_2/(N_2+Ar)$) in the sputtering and RTA-temperature (T_R).

In this paper, the R_N and T_R dependence of the ϕ_{TiN} and its impact on the device performance are systematically investigated by fabricating sputtered TiN gate MOS capacitors and MOSFETs.

2. RTA-temperature dependence of TiN gate work function

A series of MOS capacitors with different gate oxide thicknesses (t_{ox}) and different TiN gates deposited by changing R_N were fabricated to investigate the ϕ_{TiN}. The sputtering pressure was kept 1 Pa [4]. RTA at different temperatures was performed for 2 s. Then, the ϕ_{TiN}'s at different T_R's are extracted from the flat band voltage (V_{FB}) versus CET plots as shown in Fig. 1. The obtained ϕ_{TiN} and fixed charge density (N_f) for R_N = 17 and 83 % are summarized in Fig. 2. It can be seen that the higher R_N offers the lower ϕ_{TiN} due to the higher nitrogen concentration in the TiN [3]. Furthermore, it is noteworthy that the ϕ_{TiN} markedly decreases with increasing T_R. To explore the origin of the ϕ_{TiN} lowering, nitrogen profiles in the gate oxide layers before and after RTA were measured by using the backside SIMS analysis as shown in Fig. 3. It is clearly noted that the nitrogen atoms are piled up in the gate oxide layer near the Si substrate during the RTA process. Since such piled nitrogen atoms must be diffused from the TiN layer at the vicinity of gate oxide, nitrogen lack should occur at the TiN close to the gate oxide. Thus, it is considered that the ϕ_{TiN} after RTA approaches to that of titanium (Ti) with a lower work function of ϕ_{Ti} = 4.14 eV [4].

3. TiN gate MOSFET fabrication

TiN gate MOSFETs were fabricated by using conventional gate-last fabrication processes. At first, heavily doped n^+ source-drain regions were formed by ion implantation. After the 4-nm-thick gate oxide formation, the 50-nm-thick TiN film was deposited by changing the R_N from 8.3 to 100 % at pressure of 1 Pa [4]. TiN gates were made by photolithography and wet etching with an APM solution ($NH_4OH : H_2O_2 : H_2O = 1 : 2 : 5$) at 60 °C. Then, a 100-nm-thick CVD SiO_2 layer was deposited on the wafers. For some wafers, RTA was performed at different T_R's and with the same time of 2 seconds. Finally, contact holes and aluminum electrodes were formed, and all wafers were sintered in a forming gas ambient at 450 °C for 30 min.

4. R_N and T_R dependence of device performance

The I_d-V_g characteristics of the fabricated MOSFETs with as-deposited (without RTA) TiN gates under the conditions of R_N = 17 and 83 % are shown in Fig. 4. It is obvious that, in the case of R_N = 83 %, the gate voltage at which the drain current begins to flow is smaller than that for R_N = 17 %. This implies that the ϕ_{TiN} for R_N = 83 % is lower than that for R_N = 17 % as predicted from the results shown in Fig. 2. However, the S-slope deteriorates from 87 to 120 mV/decade with increasing R_N from 17 to 83 %. Figure 5 summarizes the measured device parameters and interface trap density (D_{it}) for the samples with different R_N's from 8.3 to 100 %. It is clear from Fig. 5 that the S-slope, gate leakage current (I_g) and transconductance (g_m) degrade with increasing R_N more than 50 %, which should be resulted from the D_{it} increment as shown in Fig. 5(b). Considering the above results and abrupt increase in I_g in the case of R_N = 8.3 % as shown in Fig. 5(b), the optimum R_N range should be 17 -50 %.

Figure 6 shows the T_R dependence of the I_d-V_g and I_g-V_g characteristics of the fabricated MOSFETs with the same TiN gate deposited at R_N = 17 %. It is noted that the I_d-V_g curve shifts to the negative direction by 0.32 V with increasing T_R from room temperature to 840 °C, while the S-slope is maintained to be 87 mV/decade without the I_g increment. The T_R dependence on the V_{th} and g_m of the MOSFETs with different gate lengths from 3 to 15 µm are summarized in Fig. 7. It is noteworthy that the V_{th} decreases with increasing T_R, while the g_m keeps almost a constant value at whole T_R range. This indicates that the V_{th} can be controlled by proper setting of the T_R, which is further supported from the T_R-independent electron mobility (μ_{eff}) data as shown in Fig. 8.

5. Conclusion

The dependence of the sputtered TiN gate work function (ϕ_{TiN}) and device characteristics on the nitrogen gas flow ration (R_N) in the sputtering and the RTA-temperature (T_R) has been systematically investigated by fabricating MOS capacitors and MOSFETs. It was experimentally found that the optimal R_N range is 17-50 %, and the ϕ_{TiN} markedly decreases with increasing T_R owing to the nitrogen diffusion out from the TiN in the RTA process. These results show that the ϕ_{TiN} can be controlled by the sputtering and RTA conditions, and are very useful for setting the proper threshold voltage (V_{th}) for lightly doped channel devices such as a FinFET.

References

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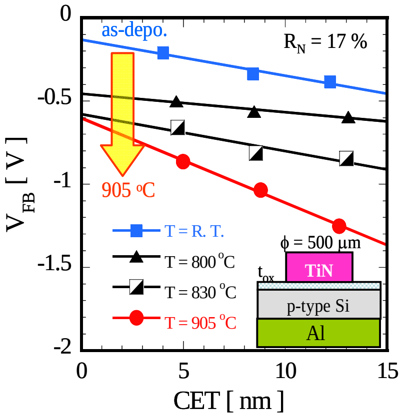

Fig. 1. Flat band voltage (V_{FB}) as a function of CET for the fabricated TiN gate MOS capacitors with the RTA-temperature as a parameter.

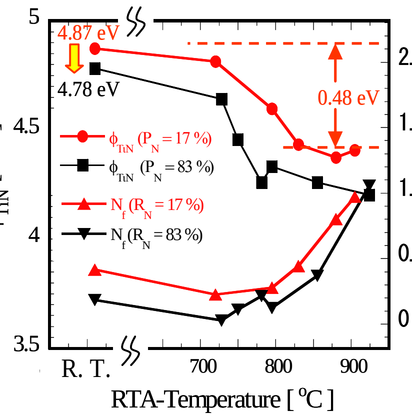

Fig. 2. RTA-temperature (T_R) dependence of the TiN work function (ϕ_{TiN}) and fixed charge density (N_f).

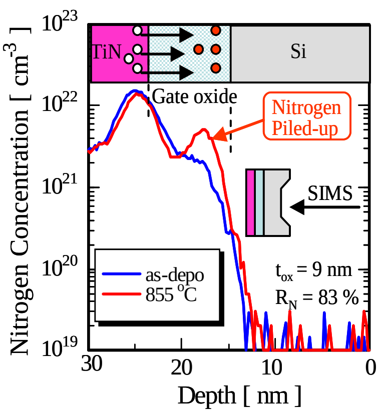

Fig. 3. Nitrogen profiles in the gate oxide layers before and after RTA obtained backside SIMS analysis.

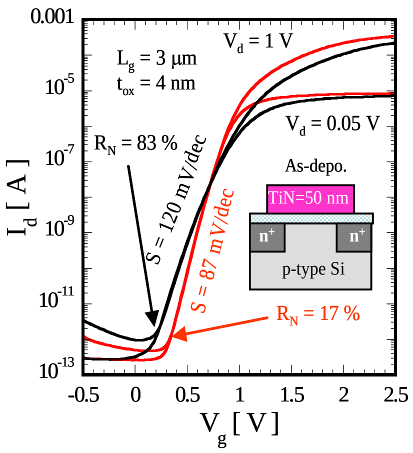

Fig. 4. I_d-V_g characteristics of the fabricated planar MOSFETs with sputtered TiN gates deposited at different R_N's of 17 and 83 %.

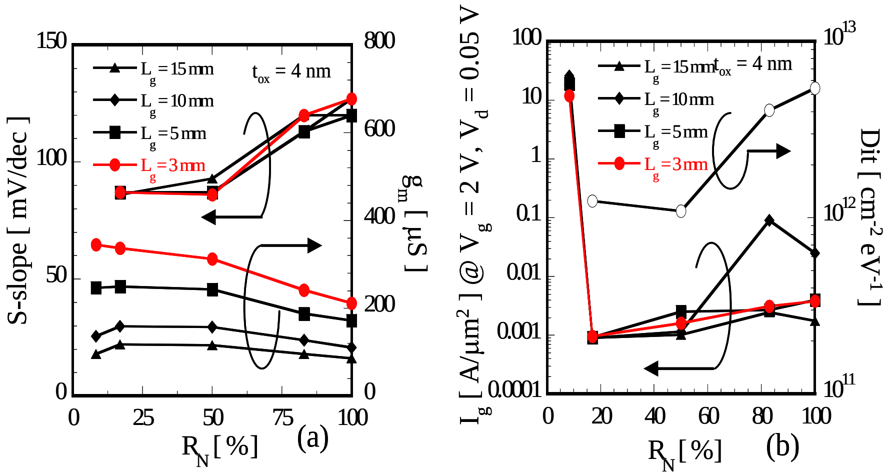

Fig. 5. R_N dependence on (a) the S-slope & g_m, and (b) the gate leakage current (I_g) & interface trap density (D_{it}) of the fabricated MOSFETs with different gate lengths from 3 to 15 μm. S-slope degradation and D_{it} increment are observed with increasing R_N more than 50 %.

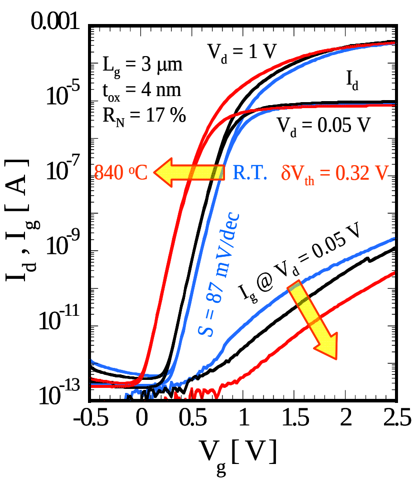

Fig. 6. I_d-V_g and I_g-V_g characteristics of the fabricated MOSFETs annealed at different T_R. The I_d-V_g curve shifts to the negative direction with increasing T_R.

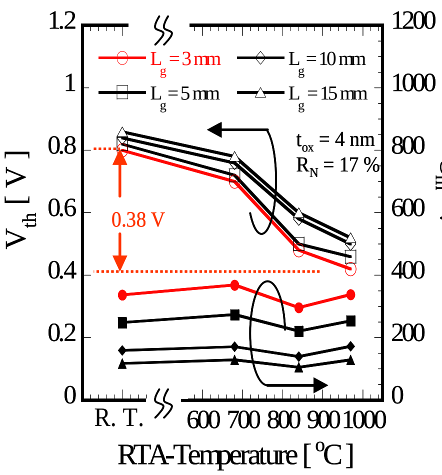

Fig. 7. RTA-temperature dependence on the V_{th} and g_m of the fabricated MOSFETs with different L_g = 3-15 μm. V_{th} decreases with increasing T_R without g_m degradation.

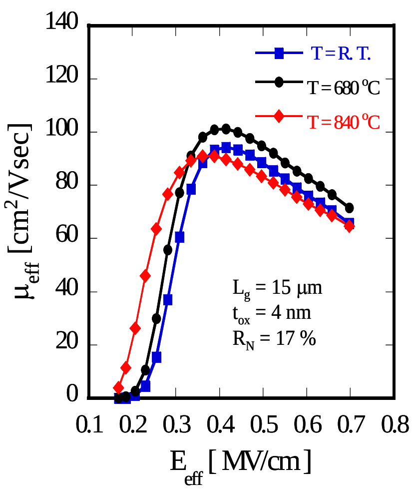

Fig. 8. Effective electron mobility (μ_{eff}) as a function of electrical field (E_{eff}) with the T_R as a parameter. No μ_{eff} degradation is observed after RTA process at different T_R's.