P-1-15

Reduced Interfacial Layer Thickness and Gate Leakage Current of ALD Grown HfAlO with TaN Gates using Chemical Oxides and Spike-Annealing

Yao-Jen Lee[1], Bo-An Tsai[2], Hsin-Yi Peng[1], Charles Pei-Jer Tzeng [3], Kuei-Shu Chang-Liao[2]
[1]National Nano Device Laboratories, Hsinchu, Taiwan
Phone: +886-3-5726100-7793. Fax: +886-3-5722715 Email:yjlee@mail.ndl.org.tw
[2] Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan
[3]Electronics Research & Service Organization, Industrial Technology Research Institute

I. INTRODUCTION

According to the ITRS, the thickness of gate oxide in 2007 will be reduced to 1.1nm. However, the nm-scale SiO_2 thin film increases leakage current drastically and cannot be used because of large power dissipation. In recent years, high-k dielectric has obtained much attention to replace SiO_2 gate insulator for the applications of ULSI [1][2]. Then, high gate capacitance or low equivalent oxide thickness thus can be achieved simultaneously with low gate currents. One of the most promising deposition techniques for high-K materials is atomic layer deposition (ALD) , since it is manufacturabe and provides excellent conformality and uniformity [3][4]. In ALD, materials are deposited layer by layer in a self-limiting fashion, allowing for inherent atomic scale control. The most widely used ALD precursors for metal oxides are metal-chlorides, such as $HfCl_4$ and $Al(CH_3)_3$. Unfortunately, metal oxide formed by a ALD using metal chloride precursors exhibits poor initial deposition on H-terminated Si[5][6], necessitating the use of an interfacial SiO_2 or Si_3N_4 layer to achieve uniform growth. However, the interfacial layer between the high-K layer and silicon substrate can have an opposing effect on this pursuit of low effective oxide thickness (E_{OT}) and low gate currents. Since an E_{OT} of less than 1 nm will soon be required, the need for an initial few monolayers of a lower dielectric constant material would be a serious drawback.

Interfacial SiO_2 layers are conventionally produced by the thermal oxidation at temperatures above 800 °C in O_2 or N_2O. The high performance of MOS devices relies on almost perfect characteristics of the Si/SiO2 interfaces. However, the serious problem is that the control of the SiO_2 thickness becomes very difficult because of the high Si oxidation rate at high temperatures.

In the present study, we will discuss the chemical oxide formed in HNO_3, SCl, and H_2SO_4. A high temperature spike annealing treatment is performed to decrease the chemical oxide thickness and then use it as the interfacial layer of high K dielectric. Characteristics of the gate stack of TaN/HfAlO/chemical oxide/Si are also compared and discussed, simultaneously.

II. Device Fabrication

The starting material was wafer of 6-in Si (100) with 15~25 Ω-cm, and it was clean using RCA methods. The first group samples are MOS devices with TaN/ SiO_2/Si structures. Gate dielectric was performed by immersing wafers in to chemical solutions (HNO_3, $NH_4OH+H_2O_2$ (SC1), and H_2SO_4). After the formation of chemical oxide layers, TaN layer was carried out in PVD system for gate electrode, and then annealed by RTA at 850 °C for 30-sec.

The second group samples are MOS devices with TaN/HfAlO/chemical oxide/Si structures. Gate dielectric was performed by immersing wafers into nitric acid solutions following by various spike-annealing (1000 °C, and 1050 °C). Then, the HfAlO films were grown by the ALD process, by alternating pulses of $HfCl_4$, H_2O and $Al(CH_3)_3$ at 300 °C. TaN layer was carried out in PVD system for gate electrode, and then annealed by RTA at 850 °C for 30-sec. Finally, Al was deposited on the backside by sputtering, and PMA treatment was performed at 400 °C in forming gas atmosphere. *I –V* characteristics were measured using an HP 4145 picoammeter. *C–V* curves, which operating frequency is 100K, were recorded with a HP4284

III. Results and Discussion

Fig. 1 shows the C–V and hysteresis curves for the TaN/ chemical SiO2 /Si(100) with the SiO_2 layer formed in HNO_3, SCl, and H_2SO_4, respectively. At the same immersion process time, the HNO_3 depicts the highest capacitance value among all splits. The hysteresis, which may limit the application because the hysteresis leads to instability of threshold voltage of MOSFETs, was defined as a difference between flat band voltages of C-V curves swept from V to -2.5 V and vice versa. From Fig. 1, the hysteresis voltage is found to be 137 mV for H_2SO_4 split, 75 mV for SCl split, and there is almost no difference for HNO_3 split.

Table I shows the oxide thickness, J_g (at $V-V_{FB}=-1V$) for the three different chemical oxides. It is interesting that HNO_3 splits have the lowest oxide thickness and J_g. Fig. 2 shows the C–V curves for MOS devices with TaN/HfAlO/chemical SiO_2 /Si(100). The interfacial SiO_2 layer was formed in HNO_3, and then annealed by high temperature spiking anneal (1000 °C, and 1050 °C). From Fig. 2, the E_{OT} and also donor-like interface state are reduced after high temperature spiking anneal as compared with ideal simulation results[7]. To compare the interfacial layer between W/ and W/O spiking anneal, high-resolution TEM pictures of TaN/ HfAlO /chemical SiO2 /Si(100) were analyzed. Fig. 3 shows TEM pictures for interfacial layer after spiking anneal in nitrogen ambient. Note that the splits with 1000 °C (Fig. 3(b)), and 1050 °C (Fig. 3(b)) spike anneal show thinner physical thickness, which was from 1nm for W/O anneal (Fig. 3(a)) to 0.7 nm for 1000 °C, and 1050 °C spike anneal. Therefore, HNO_3 chemical oxide could be effectively reduced by high temperature spike anneal. Fig. 4 shows the C–V and hysteresis curves for the TaN/ HfAlO /chemical SiO_2 /Si samples with (a) control (b) spiking anneal at 1050 °C. There is almost no hystersis difference for HNO_3 splits with or W/O high temperature anneal. Therefore, instability of threshold voltage could be ignored.

Fig. 5 shows gate leakage currents-voltage characteristics. The splits with high temperature spike anneal show higher gate current due to its thinner interfacial oxide thickness. However, the leakage current was suppressed around gate voltage around 0 V. This is because the interface states were suppressed after spike anneal. Fig. 6 shows stress induced leakage current (SILC) characteristics of the TaN/ HfAlO /chemical SiO2 /Si. SILC is defined as the increase in leakage current after stress {Jg(T)-Jg(0)} divided by leakage current of a fresh device (J g(0)). Compared to the splits W/O spike anneal, negligible SILC for the splits with high temperature spike anneal is observed.

IV. Summary

Chemical oxidation of Si by different chemical is investigated in view of its application to gate oxides. HNO_3 oxide shows the thinnest gate oxide and lowest leakage current among all chemical oxide splits. Furthermore, the method of high temperature spike anneal not only reduce the thickness of HNO_3 chemical oxide, but also suppress the gate leakage current and SILC due to reduced donor-like interface traps.

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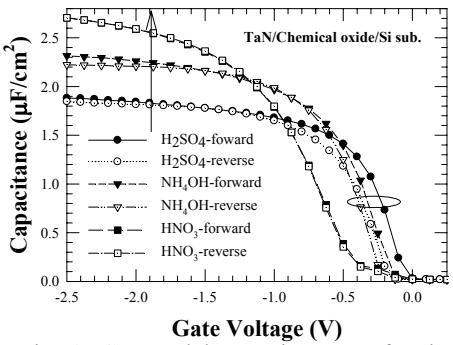

Fig. 1. C–V and hysteresis curves for the TaN/ chemical SiO2 /Si(100) with the SiO_2 layer formed in HNO_3, SCI, and H_2SO_4, respectively.

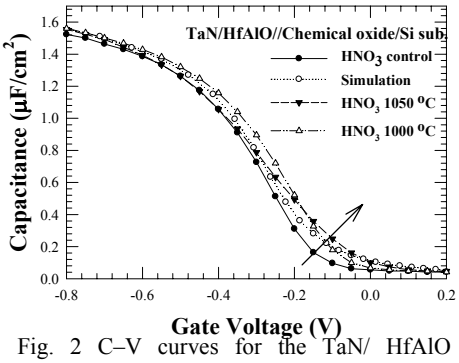

Fig. 2 C–V curves for the TaN/ HfAlO /chemical SiO2 /Si(100). The interfacial SiO_2 layer formed in HNO_3, and then annealed by high temperature spiking anneal (1000 °C, and 1050 °C).

Sample	Chemical oxide	EOT	Jg(A/cm²) at V-Vfb=-1 V
1	H_2SO4	14.5Å	6.212
2	SCI	10.5Å	11.815
3	HNO_3	9Å	4.2881

Table I. Oxide thickness, J_g (at $V\text{-}V_{FB}$=-1V) for the three different chemical oxide.

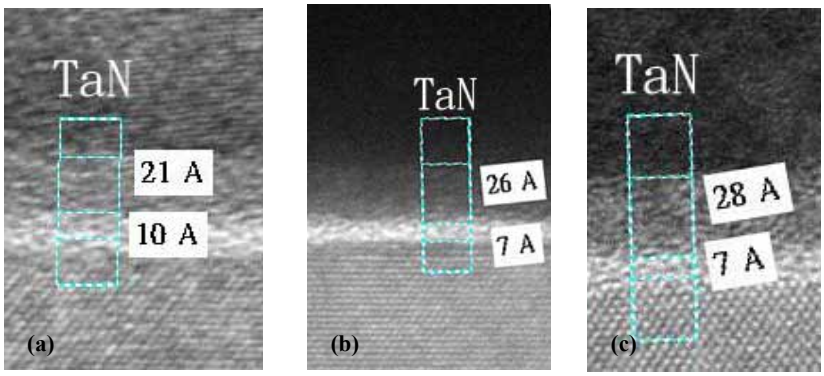

Fig. 3 TEM pictures for interfacial layer, (a) Control sample: W/O anneal (b) Spike anneal: 1000 °C (c) Spike anneal: 1050 °C

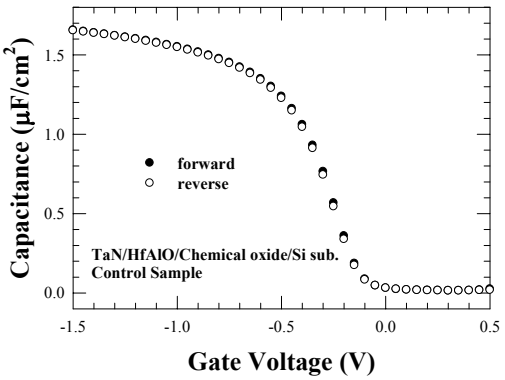

Fig.4(a). C–V and hysteresis curves for the TaN/ HfAlO /chemical SiO2 /Si control sample.

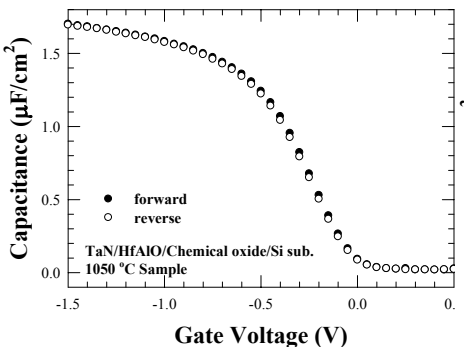

Fig.4(b). C–V and hysteresis curves for the TaN/ HfAlO /chemical SiO2 /Si sample with 1050 °C spiking annealing.

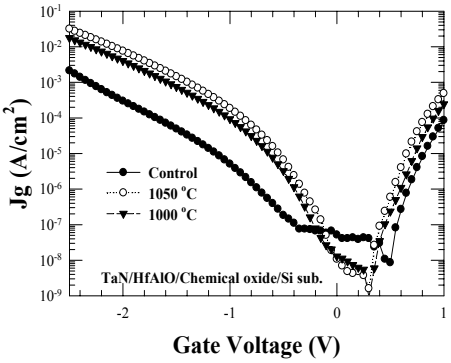

Fig.5. Gate leakage currents versus voltage characteristics for all split samples.

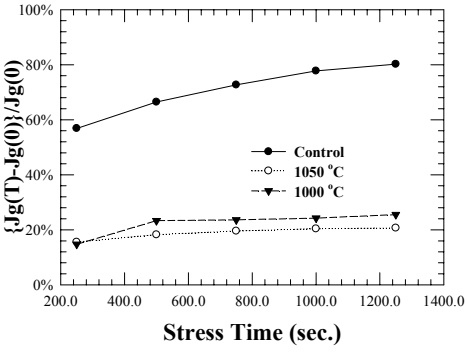

Fig.6. SILC characteristics of the TaN/ HfAlO /chemical SiO2 /Si(100). SILC is defined as the increase in leakage current after stress {Jg(T)-Jg(0)} divided by leakage current of a fresh device (J g(0)).