Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 366-367

P-1-22

Schottky Barrier Height Modulation for Nickel Silicide on n-Si (100) using Antimony (Sb) Segregation

Hoong-Shing Wong, Lap Chan, Ganesh Samudra, Yee-Chia Yeo

Silicon Nano Device Lab., Department of Electrical and Computer Engineering, National University of Singapore, 117576, Singapore.
Phone: +65 6516-2298, Fax:+65 6779-1103, Email: yeo@ieee.org

1. INTRODUCTION

Beyond the 32 nm technology generation, there are increasing concerns about the impact of parasitic series resistance R_{series} on CMOS device performance [1]. It is reported that the silicide-diffusion contact resistance R_{csd} contributes up to ~40% of the total R_{series} [2]. In heavily doped source/drain region, R_{csd} is determined by the effective Schottky Barrier (SB) height, which strongly depends on the active dopant concentration at the silicide/Si interface [3]. In this paper, we report a new method of SB height modulation for NiSi on n-Si (100) using Antimony (Sb) segregation. Devices with Sb segregation could achieve ~5 orders of magnitude increase in the reverse current I_r and an almost ideal unity value of rectification ratio R_C as compared to a device without Sb. The I_r show less degradation when device active area is reduced and annealing temperature is increased. We also show that effective SB height modulation using Sb segregation is also achievable with thin NiSi.

2. EXPERIMENTS

Figure 1 shows the process flow of fabricating low SB height devices using Sb segregation. N-type bulk Si (100) wafers with a resistivity of 4-8 Ω.cm were used for the fabrication. After standard wafer cleaning steps, 400 nm thick SiO_2 layer was grown using thermal oxidation. A reverse-isolation mask was used for active definition, and the SiO_2 was etched to form device active regions. Sb with a thickness t_{Sb} ranging from 5 to 15 nm was deposited, followed by a Ni layer of thickness t_{Ni} 30 nm in an e-beam evaporation system. Prior to silicidation, the Sb appears as an interlayer sandwiched between Ni and n-Si as shown in Figure 1. A one-step rapid thermal annealing (RTA) in a nitrogen ambient was used for the Ni silicidation process. Various RTA temperatures were used. The unreacted Ni and Sb were removed by using a wet etchant comprising H_2SO_4 and H_2O_2 with a volume ratio of 4:1. A layer of Al (200 nm) was deposited on backside of the wafers for ohmic contact. The structural properties of NiSi formed on n-Si (100) with Sb segregation were studied by Secondary Ion Mass Spectrometry (SIMS) and X-Ray Diffraction (XRD).

3. RESULTS AND DISCUSSION

Figure 2 shows the room temperature I-V characteristics for devices with and without Sb interlayer. All the devices were annealed at 500°C. The reverse current increases as the Sb interlayer thickness is increased from 5 nm to 15 nm. The highest reverse current is obtained from devices with t_{Sb} of 15 nm, which is ~5 orders of magnitude higher than device without Sb. Rectification ratio R_C could be used to evaluate SB height modulation. R_C is defined as the ratio of forward current I_f at V_f of 0.5 V to reverse current I_r at V_r of -0.5V of the device. Higher effective SB height leads to higher R_C value and R_C should be 1 for an ideal ohmic contact. Figure 3 illustrates the R_C modulation as a function of t_{Sb}. The results show that R_C value could be widely varied by changing t_{Sb}. Devices with t_{Sb} of 15 nm annealed at 500°C show an almost ideal value of R_C. Figure 4 shows the SIMS depth profile of Si, Ni, and Sb for a device with t_{Sb} of 15 nm which was annealed at 500°C. Peak Sb concentration is located at the NiSi/Si interface region, indicating that Sb segregated at NiSi/Si interface. Sb segregation at the NiSi/Si interface is believed to lead to effective SB height modulation.

Figure 5 shows R_C as a function of applied voltage for device with t_{Sb} of 15 nm and annealed at 500°C. R_C is reduced when the applied voltage is reduced from 1.0V to 0.4V. Figure 6 shows the normalized reverse current density J_r as a function of device active area. The J_r, which is measured at V_r = -1.0V, of the devices is normalized with J_r obtained from the devices with largest device active area. The J_r of devices with Sb segregation show enhancement compare to devices without Sb as the device area reduced. We believe that this result is consistent with reduced effective SB height of the devices. Figure 7 plots the dependence of I_r on annealing temperatures. No I_r degradation is observed for devices with Sb segregation as the annealing temperature increases from 500°C to 700°C, suggesting good thermal stability. Figure 8 shows the XRD analysis for devices with t_{Sb} of 15 nm and annealed at (a) 700°C, (b) 600°C, and (c) 500°C. No change in NiSi structural properties was detected when the annealing temperature increases from 500°C to 700°C. Figure 9 reveals that Sb segregation could be applied on thin NiSi (t_{Ni} of 10 nm) and the R_C values of the devices are near the ideal unity value. This shows viability of Sb segregation for thin NiSi formed on n-Si (100) which is critical for source/drain engineering and integration in sub-32 nm CMOS technology.

4. CONCLUSION

We demonstrated a new method of SB height modulation for NiSi on n-Si (100) using Sb segregation. An almost ideal rectification ratio R_C of close to unity was achieved. Device with Sb segregation also shows less degradation than device without Sb when device active area is reduced and annealing temperature is increased. Viability of Sb segregation using thin NiSi is also reported.

ACKNOWLEDGEMENT

This work was supported by the Nanoelectronics Research Program, Agency for Science, Technology, & Research, Singapore.

REFERENCES

[1] J. W. Sleight *et al*., *IEDM Tech. Dig*., pp. 851, 2006.
[2] S. D. Kim *et al*., *IEEE TED* 49, pp.467, 2002.
[3] S. M. Sze., *Physics of Semiconductor Devices,* 1981.

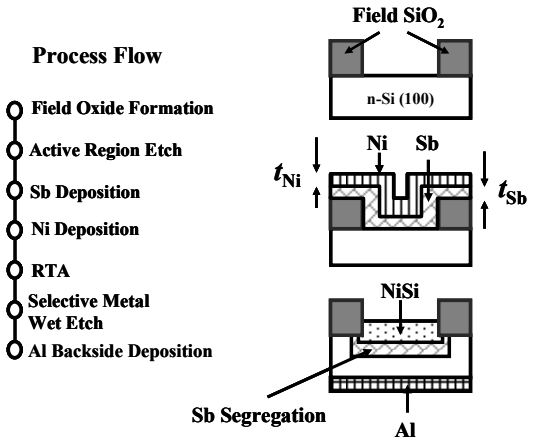

Fig. 1. Process flow for fabricating low Schottky barrier height devices using Sb segregation.

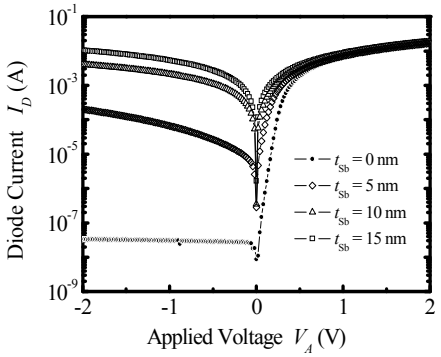

Fig. 2. Current-voltage characteristics at room temperature for NiSi on n-Si (100) devices with and without Sb interlayer. All devices were annealed at 500°C. Schottky barrier modulation for NiSi on n-Si (100) is observed when t_{Sb} is varied.

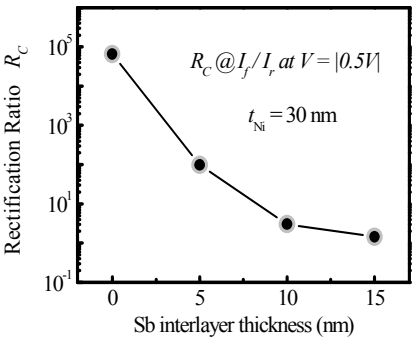

Fig. 3. Rectification ratio R_C (I_f/I_r) as a function of t_{Sb}. R_C almost reach the ideal unity value for t_{Sb} of 15 nm and t_{Ni} oof 30 nm annealed at 500°C

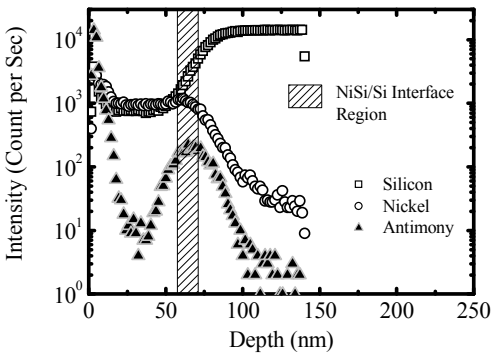

Fig. 4. SIMS depth profiles of Si, Ni, and Sb for a device with t_{Sb} of 15 nm and t_{Ni} of 30 nm. The device was annealed at 500°C. Sb is segregated at the NiSi/Si interface region.

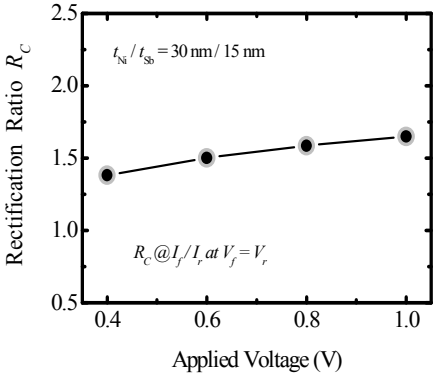

Fig. 5. R_C as a function of applied voltage for devices with Sb segregation. R_C slightly reduced when applied voltage is reduced from 1.0V to 0.4V.

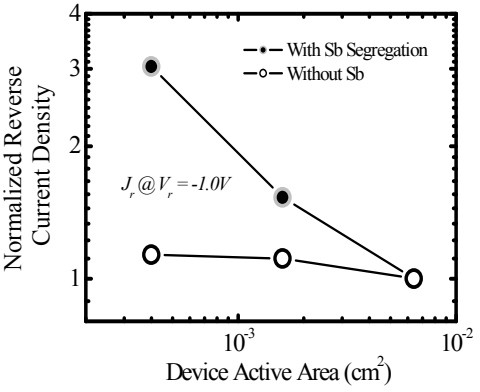

Fig. 6. Normalized reverse current density as a function of device active area. Devices with Sb segregation show J_r enhancement compare to device without Sb when device active area is reduced.

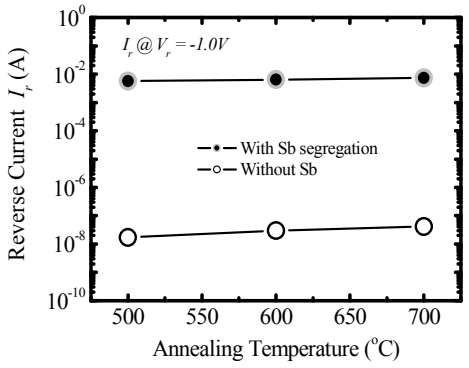

Fig. 7. Dependence of reverse current on annealing temperature for devices with Sb segregation and without Sb. No significant degradation is observed when the annealing temperatures is increased from 500°C to 700°C.

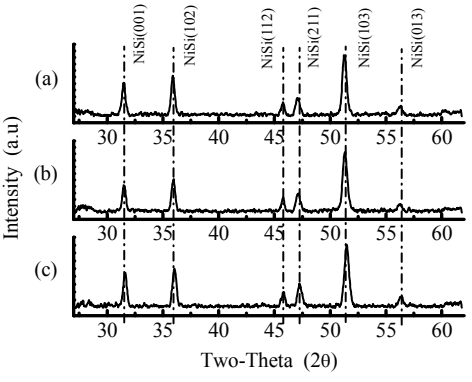

Fig. 8. XRD profiles of Ni/Sb/n-Si (100) after RTA at (a) 700°C, (b) 600°C, and (c) 500°C. No degradation of NiSi structural properties are observed when the anneal temperature increased from 500°C to 700°C.

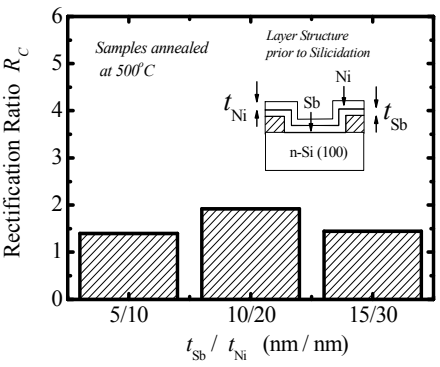

Fig. 9. Rectification Ratio R_C dependence on t_{Sb}/t_{Ni} ratio. Schottky barrier modulation for thin NiSi using Sb segregation could be achieved by reducing the t_{Sb} thickness.