Schottky Barrier Height Modulation for Nickel Silicide on n-Si (100) using Antimony (Sb) Segregation

Hoong-Shing Wong, Lap Chan, Ganesh Samudra, Yee-Chia Yeo
Silicon Nano Device Lab., Department of Electrical and Computer Engineering, National University of Singapore, 117576, Singapore.
Phone: +65 6516-2298, Fax:+65 6779-1103, Email: yeo@ieee.org

1. INTRODUCTION

Beyond the 32 nm technology generation, there are increasing concerns about the impact of parasitic series resistance $R_{	ext{series}}$ on CMOS device performance [1]. It is reported that the silicide-diffusion contact resistance $R_{	ext{cnt}}$ contributes up to ~40% of the total $R_{	ext{series}}$ [2]. In heavily doped source/drain region, $R_{	ext{cnt}}$ is determined by the effective Schottky Barrier (SB) height, which strongly depends on the active dopant concentration at the silicide/Si interface [3]. In this paper, we report a new method of SB height modulation for NiSi on n-Si (100) using Antimony (Sb) segregation. Devices with Sb segregation could achieve ~5 orders of magnitude increase in the reverse current $I_r$ when the annealing temperature increases from 500°C to 700°C. Figure 5 reveals that Sb segregation could be applied on thin NiSi. Sb segregation also shows less degradation than device without Sb as the device area increased. We believe that this result is consistent with reduced effective SB height of the devices.

2. EXPERIMENTS

Figure 1 shows the process flow of fabricating low SB height devices using Sb segregation. N-type bulk Si (100) wafers with a resistivity of 4-8 $\Omega \cdot \text{cm}$ were used for the fabrication. After standard wafer cleaning steps, 400 nm thick SiO$_2$ layer was grown using thermal oxidation. A reverse-isolation mask was used for active definition, and the SiO$_2$ layer is etched to form device active regions. Sb with a thickness $t_{\text{Sb}}$, ranging from 5 to 15 nm, was deposited followed by a Ni layer of thickness $t_{\text{Ni}}$. Various RTA temperatures were used. The unreacted Ni and Sb were removed by using a wet etchant comprising H$_2$SO$_4$ and H$_2$O$_2$ with a volume ratio of 4:1. A layer of Al (200 nm) was deposited on backside of the wafers for ohmic contact. The structural properties of NiSi formed on n-Si (100) with Sb segregation were studied by Secondary Ion Mass Spectrometry (SIMS) and X-Ray Diffraction (XRD).

3. RESULTS AND DISCUSSION

Figure 2 shows the room temperature I-V characteristics for devices with and without Sb interlayer. All the devices were annealed at 500°C. The reverse current increases as the Sb interlayer thickness is increased from 5 nm to 15 nm. The structural properties of NiSi formed on n-Si (100) with Sb segregation were studied by Secondary Ion Mass Spectrometry (SIMS) and X-Ray Diffraction (XRD).

4. CONCLUSION

We demonstrated a new method of SB height modulation for NiSi on n-Si (100) using Sb segregation. An almost ideal rectification ratio $R_\circ$ of close to unity was achieved. Device with Sb segregation also shows less degradation than device without Sb when device active area is reduced and annealing temperature is increased. Viability of Sb segregation using thin NiSi is also reported.

ACKNOWLEDGEMENT

This work was supported by the Nanoelectronics Research Program, Agency for Science, Technology, & Research, Singapore.

REFERENCES

Intensity (Count per Sec)

Wet Etch

Active Region Etch

Selective Metal

Al Backside Deposition

Field Oxide Formation

RTA

Sb Deposition

Ni Deposition

RTA

Selective Metal

Wet Etch

Al Backside Deposition

Sb Segregation

Field SiO$_2$

n-Si (100)

Ni

Sb

NiSi

Sb

n-Si (100)

Fig. 1. Process flow for fabricating low Schottky barrier height devices using Sb segregation.

Fig. 2. Current-voltage characteristics at room temperature for NiSi on n-Si (100) devices with and without Sb interlayer. All devices were annealed at 500°C. Schottky barrier modulation for NiSi on n-Si (100) is observed when $t_{\text{Sb}}$ is varied.

Fig. 3. Rectification ratio $R_C (I_r/I_f)$ as a function of $t_{\text{Sb}}$. $R_C$ almost reach the ideal unity value for $t_{\text{Sb}}$ of 15 nm and $t_{\text{oof}}$ of 30 nm annealed at 500°C.

Fig. 4. SIMS depth profiles of Si, Ni, and Sb for a device with $t_{\text{Sb}}$ of 15 nm and $t_{\text{oof}}$ of 30 nm. The device was annealed at 500°C. Sb is segregated at the NiSi/Si interface region.

Fig. 5. $R_C$ as a function of applied voltage for devices with Sb segregation. $R_C$ slightly reduced when applied voltage is reduced from 1.0V to 0.4V.

Fig. 6. Normalized reverse current density as a function of device active area. Devices with Sb segregation show $J_r$ enhancement compared to device without Sb when device active area is reduced.

Fig. 7. Dependence of reverse current on annealing temperature for devices with Sb segregation and without Sb. No significant degradation is observed when the annealing temperatures is increased from 500°C to 700°C.

Fig. 8. XRD profiles of Ni/Sb/n-Si (100) after RTA at (a) 700°C, (b) 600°C, and (c) 500°C. No degradation of NiSi structural properties are observed when the anneal temperature increased from 500°C to 700°C.

Fig. 9. Rectification Ratio $R_C$ dependence on $t_{\text{Sb}}/t_{\text{oof}}$ ratio. Schottky barrier modulation for thin NiSi using Sb segregation could be achieved by reducing the $t_{\text{Sb}}$ thickness.