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Top-view imaging of 65nm gate length metal-oxide-semiconductor field effect transistors by scanning capacitance microscopy

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1. Introduction

Nowadays, it is essential for the remarkably miniaturized metal-oxide-semiconductor field effect transistors (MOSFETs) to achieve the expected performance by optimizing the two-dimensional (2-D) carrier profiles. The cross-sectional analysis of device structure by scanning capacitance microscopy (SCM) [1] with their advanced variations [2] and conductive atomic force microscopy [3] are widely used for the carrier concentration diagnostics with high-spatial resolution. The cross-sectional measurements of MOSFET, however, yields only the limited information of device parameters such as channel length (L_{met}) or extension-gate overlap length (L_{ov}) of specific section. Therefore, some prier works have tried to clarify the carrier profiles along the device-width direction [4,5]. In this work, we have demonstrated our SCM application to evaluate the channel structure of MOSFET through the "top-view" imaging.

2. Experiment

Figure 1 illustrates the schematic diagram of our SCM measurement. To avoid the photoperturbation effect arising from the optical deflection setup [6], a quartz resonator (TF) was employed as a force senser and sharpened bulk tungsten for a conductive probe [7,8]. An AC modulation bias (V_{ac}) and DC offset bias (V_{dc}) was supplied to the sample, while the SCM probe was grounded through the capacitance sensor. Our SCM simultaneously yields three kinds of images of the topography, conventional bias modulated capacitance (dC/dV), and differential static capacitance (ΔC) [9]. For the semiconductor sample measurement, the dC/dV signal was from the modulation of the carrier depletion layer just beneath the SCM probe tip. On the other hand, the ΔC signal directly senses the static capacitance between probe tip and the sample hence it can apply for the dielectric film measurement as well as the semiconductor samples. With the use of ΔC imaging, a single electron trap within high-k film was successfully observed [10].

MOSFET samples with 65nm gate length were fabricated by the standard production process with source/drain extension (SDE) implantation. HF etching was used to remove the gate structures so that the channel surface was exposed. Before the measurements, samples were air-baked, and illuminated by vacuum ultra-violet (VUV) light to make a thin, uniform oxide layer on the surface. All of the experiments were performed in high vacuum (~10^{-4} Pa) environment at room temperature.

3. Results and Discussion

Figures 2(a), (b), and (c) are a set of simultaneously obtained images of p-MOSFET under bias conditions $V_{ac}=0.4V_{P\text{-}P}$ at a frequency of 500 kHz and $V_{dc}=0$V. The topography image of Fig. 2(a) shows the convex surface, and there seems no obvious contrast in the dC/dV image of Fig. 2(b). On the other hand, the ΔC image of Fig. 2(c) shows dark strips on the both side of channel region. Figure 2(d) is the ΔC image from the 2nd scanning from the reverse direction on the same area as in (a)~(c). The observed strips have practically the same contours as that of Fig. 2(c). Therefore, these observed strips in Figs. 2(c) or (d) are not caused by artifacts from the measurement setup. Figure 3 indicates the cross-sectional line profiles along the line L-L' in Figs. 2(a) and (c), together with the cross-sectional TEM image of gate structure with same scale. As shown in Fig. 3, the slow hillock in the topography profile denotes the trace of gate structure, and two dents seen in the ΔC profile correspond to the dark strips of Fig. 2(c). Figures 4(a)~(c) present an intuitive explanation of the ΔC profile. Fig. 4(a) shows schematic view of device structure and (b) illustrates the distribution of carrier concentration of the active region in a substrate. Carrier concentration varies from SDE to channel region, and reaches its minimum at the locus of the p-n junction. And Fig. 4(c) indicates the corresponding ΔC profile. By the nature of its means of detection, the ΔC signal detects the depletion capacitance (C_{dep}) within the Si substrate [10]. Together with the former results of bias dependence [4.5], the dent in the ΔC profile is considered to correspond to the locus of the p-n junction. Therefore the distance between two minimum of the dents in the ΔC profile corresponds to L_{met}, and the strips in the ΔC image can be assessed to the width of carrier depletion region within the channel. The channel region is expected to be entirely depleted, because simultaneously obtained dC/dV image of Fig. 2(b) shows only slight contrast. This suggests that the carrier density of channel region is too low to yield the enough dC/dV signal sensitivity [11][12].

Fig. 5 shows the estimated gate length (L_g) and L_{met} from Figs. 2(a) and (c) for 20 points plotted along the channel-width direction. And Fig. 6 summarizes the correlation diagram between L_{met} and corresponding L_g. It can be said from Figs. 5 and 6 that each value of L_{met} is moderately related to $L_{g,}$, however, the spatial fluctuation of L_{met} is not entirely consistent with that of L_g. These results suggest that the fluctuation of L_{met} might be determined not only by the line edge roughness of gate electrode but also by the dopant diffusion.

4. Conclusion

We have applied our SCM to visualize the channel structure of 65 nm gate length p-MOSFET through the "top-view" imaging. The spatial variation of obtained L_{met} is not entirely consistent with line edge roughness of gate electrode, which suggests that the fluctuation of L_{met} might be determined not only by the line edge roughness of gate electrode but also by the diffusion length fluctuation of dopant.

Acknowledgements

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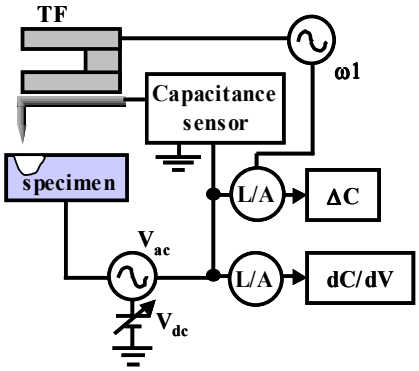

Fig. 1. Schematic diagram of measurement setup of our SCM.

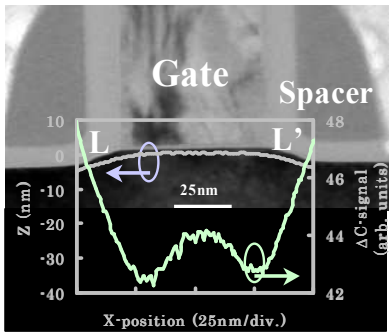

Fig. 3. Topography and ΔC profiles along L-L' in Fig. 2(a) and (c), together with the cross-sectional TEM micrograph of device.

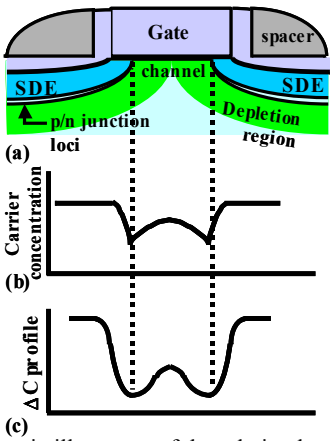

Fig. 4. Schematic illustraton of the relation between device structure, carrier profile, and resultant ΔC profile.

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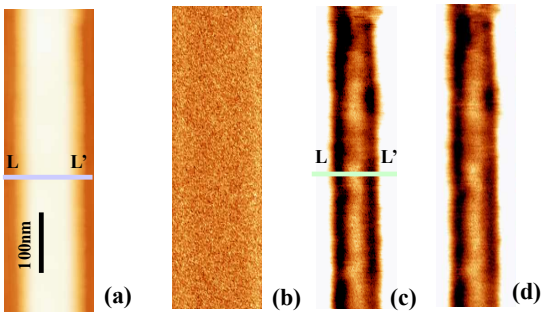

Fig. 2. A set of SCM images of p-MOSFET simultaneously obtained (a) Topography, (b) dC/dV image, (c) ΔC image, and (d) ΔC image obtained from the reverse direction scanning. Showing areas are 150 nm x 500 nm in each images.

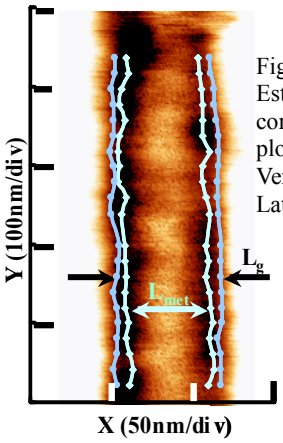

Fig. 5.
Estimated channel length (L_{met}) and corresponding gate length (L_g) plotted along the channel-width direction.
Vertical scale (Y); 100nm/div
Lateral scale (X); 50nm/div

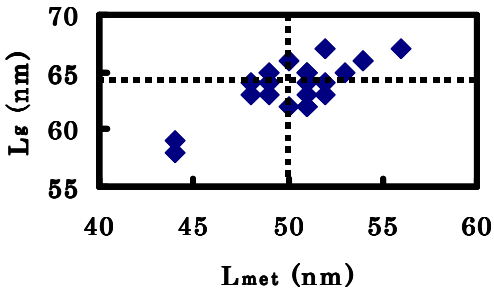

Fig. 6. Correlation diagram between L_{met} and corresponding L_g. The dotted line denotes average value of L_{met} (50nm) and L_g (64nm).