P-1-3

A lithographical method by oxidization through a conductive template in contact with a silicon substrate mediated by a thin water layer

Chi-Hsiang Hsieh¹, Jiunn-Der Liao^{1,2}, Chang-shu Kuo² Chao-Yu Huang¹, Bo-Hsiung Wu¹

¹Center for Micro/nano Science and Technology, National Cheng Kung University, Tainan, Taiwan 701

²Department of Materials Science and Engineering, National Cheng Kung University, Tainan, Taiwan 701

*Phone: +886-6-2757-575 ext. 31385 E-mail: lausie@mail.mina.ncku.edu.tw

Abstract

The oxidization imprint process is a non-thermal, non-optical, non-irradiation technique that utilizes a charged conductive template in contact with a silicon substrate. When the oxidization occurs on the imprint area, a dense oxidization on the silicon substrate can be formed, which is resistant to 20% KOH aqueous solution. In this study, the width of the imprint patterns, the space between the oxidized patterns and the etched depth are very distinguishable and are associated with the dimension of the pristine template. It reveals that the oxidization imprint process is promising to prepare anti-etching patterns for lithography with low cost, high yield and high throughput.

1. Introduction

Optical lithography encountered the tremendous problem of the inherent limitation and high tool price. Recent lithographical methods using e-beam, focus ion beam or scanning probe can achieve high resolution, whereas they can not meet the industrial demand and are limited by their low processing speed. Recent imprint technique has improved a wide-range assembly for industry applications with low cost, high resolution and high performance. It challenges the advanced optical lithography such as X-ray lithography, extreme ultraviolet lithography. These imprint techniques are hot embossing [1], soft imprint [2], UV curing [3,4], laser associated direct imprint [5]. The mechanics are hot, chemical reaction, UV light and laser respectively. They provide a new way for the manufacture of low cost and high resolution. In some imprint techniques, resist layer is the spreading polymer. The sticking problem is a puzzle in the processing of the drawing template. The template fabrication and lifetime are also the important factors for the application on the industry. Therefore, the development of imprint has a tendency of room temperature and low pressure on processing. In this work, we apply a low voltage on a conductive patterned template that is expected to produce the oxidization on the imprint silicon substrate. The experiment is performed at room temperature without loading during processing. The oxidized silicon substrate should be resistant to etching solution and to reduce template/ substrate sticking problem. The aim is to simply the lithographical process, simultaneously, to perform the process with low cost, high yield and high throughput.

2. Material and method

In this oxidization imprint process, one template was fabricated on the silicon substrate with micro-scale line patterns using lithographical method on it. For the conductive purpose, the template was deposited a platinum film using e-beam sputtering method. The film thickness was estimated around 60 nm. Two Cu plates for loading and charging were prepared. A silicon substrate for the oxidation imprint was placed on the lower Cu plate. Before imprinting, a layer of water was absorbed and spread on the silicon substrate. The as-prepared template was then placed upon the silicon substrate, followed by the load of the upper Cu plate. The schematic of the experimental set-up was shown in Fig. 1. These two Cu plates were assembled as electrodes and loads with pressure. The conductive wire connected the plates with an electric power, which supplied with the lectric pulse voltage. The silicon substrate surface (100) is n-type doped with Boron and the piece resistivity is about $1 \sim 10 \Omega$ -cm. The silicon substrate and the template were regarded as the anode and the cathode respectively. When a voltage bias is applied, the silicon substrate surface tends to be depassivated. The formation of O2- and OHions is anticipated, while silicon oxide is formed on the substrate surface [6].

The applied pulse voltages for the imprint process were -10V and 10V and kept 0.4 and 0.1 sec respectively. It was to avoid the charges from accumulating on the substrate surface. There were 30 cycles of pulse voltages executed for one experiment. After the oxidization imprint process, the samples were etched by 20% KOH aqueous solution for



Fig. 1 The schematic of the experimental set-up: (1) the upper Cu plate, (2) the template as the mold, (3) the silicon substrate for the oxidation imprint, (3) the lower Cu plate as the holder.

5 min at room temperature.

3. Discussion

The oxidization imprint process is performed at room

temperature, while the layer of water absorbed on the silicon substrate acts as the inter-mediator of this process. In the process of water molecules spreading on the substrate surface, the quantity as well as the average thickness is still difficult to be determined. However a full coverage of water film between the template and the substrate surface is necessary for the oxidization imprint process. Followed by the etching process, a Nanofocus image of the etched pro-



Fig. 2 (a) Nanofocus image of the oxidized silicon substrate: line patterns of around 20 μ m were formed by the oxidization imprint process. (b) By line profile crossing over the oxidized pattered in (a), an etched depth of about 60 nm was determined.

file was assessed. In Fig. 2, line patterns of around 20 μ m were formed by the oxidization imprint process, while a distance of around 60 μ m between the line patterns was resulted. The space scale of the line profile is comparable with size of the template. By line profile crossing over the oxidized pattern in (a), an etched depth of about 60 nm was determined. The result demonstrated that an electrochemical reaction was occurred that was associated with the oxidization on the silicon substrate. From depth profile analysis, an etching rate using 20% aqueous KOH of about 16 nm per minute at room temperature was estimated.

It is assumable that the electrical field is stretched over the silicon substrate, as illustrated in Fig. 3. Nevertheless, the density of the electrical field may decay dramatically away from the oxidization imprint. Therefore the interface of the template or the mold in contact with the silicon substrate can be divided into four parts when the bias voltage is applied: (1) the template or the mold induced electrical field, (2) the outermost surface of the decayed electrical field as a water bridge, (3) a dense SiO₂ formation created by the oxidization of the silicon substrate, and (4) a trace SiO₂ formation owing to the interaction or the transmission of the electrical field mediated by the water layer. The electrical field induced area is resistant to the 20% KOH aqueous solution. The width of the area is close to the width of the template, while the depth of the area is well distinguishable. It reveals that the oxidization imprint process has been created, whereas the trace formation of oxidization on the silicon substrate does not resist to the 20% KOH aqueous solution.



Fig. 3: Illustration of the electrical field stretched over the silicon substrate: the density of the electrical field may decay dramatically away from the oxidization imprint. The interface of the template or the mold in contact with the silicon substrate can be divided into four parts when the bias voltage is applied.

4. Conclusion

The oxidization imprint process is feasible through a charged template in contact with the silicon substrate. The imprint area, where a dense oxidization on the silicon substrate is generated, is close to the width of the template. The oxidized area is resistant to 20% KOH aqueous solution. The space between the oxidized patterns is distinguishable and is associated with that of the pristine template. It is therefore achievable to prepare an anti-etching pattern using this oxidization imprint process.

Acknowledgements

We would like to express our sincere thanks to the Center for Micro/Nano Science and Technology, National Cheng Kung University for providing the facilities.

Reference

- S. Y. Chou, P. R. Krauss, and P. J. Renstrom, Applied Physics Letters 67(21), 3114-3116, 1995.
- [2] Younan Xia and George M. Whitesides, Annu. Rev. Mater. Sci. 28, 153–84, 1998.
- [3] M. Bender, M. Otto, B. Hadam, B. Spangenberg, and H. Kurz, Microelectronic Engineering Vol.53, 233–236, 2000.
- [4] M. Otto, M. Bender, B. Hadam, B. Spangenberg, and H. Kurz, Microelectronic Engineering Vol. 57-58, 361–366, 2001.
- [5] Stephen Y. Chou, Chris Keimel, and Jian Gu, Nature Vol.417 (6891): 835-837 2002.
- [6] T. H. Fang Microelectronics Journal, Vol. 35, 701-707, 2004.