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Physical and Electrical Properties of Addition Ti into Er_2O_3 Gate Dielectrics

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1. Introduction

According to the International Technology Roadmap for Semiconductors (ITRS), the gate oxide thickness less than 12Å will be required for 65 nm complementary metal oxide semiconductor (CMOS) devices [1]. Thinner silicon dioxide (< 12 Å) cannot applied for gate dielectrics because of its low dielectric constant and high direct tunneling current leading to the limitation of low power devices. However, lanthanide oxide materials, such as La_2O_3, Pr_2O_3 and Er_2O_3 [2-4], are attractive candidates for alternative gate dielectrics based on thermodynamic consideration because they possess moderately high dielectric constants and have high conduction band offset with silicon.

In this work, we studied on the structural and electrical characteristics of thin Er_2TiO_5 film as the gate dielectric deposited on Si substrate by reactive RF sputtering. The crystalline structure, chemical binding status, and electrical characteristics upon thermal annealing were investigated.

2. Experiments

The p-type Si (100) wafer was cleaned by standard RCA clean and dipped in dilute HF solution. A ~8 nm Er_2O_3 film was grown on Si substrate by reactive RF sputtering and, then a ~4 nm Ti thin film was added on the Er_2O_3 film. The samples were treated by rapid thermal annealing for 30 seconds in an O_2 ambient at 600-800 °C to form titanium erbium oxide structure. The Al metal gate of 300 nm was deposited by thermal evaporator. The gate of the capacitor was defined by lithographically. Finally, all samples were backside Al deposition. The key process flow was shown in Fig. 1. The electrical and reliability characteristics of the metal oxide were measured by HP 4156C.

3. Result and Discussion

The XRD data of Er_2TiO_5 dielectrics for various anneal conditions are depicted in Fig. 2. A single weak Er_2TiO_5 (102) peak in the spectrum of 600°C sample indicates an amorphous or badly crystallized Er_2TiO_5 structure. It is obvious that no peak was observed in the sample after annealing at 700 °C, suggesting that Er_2TiO_5 remains amorphous. However, one strong (102) peak was found in the diffraction patterns of the film annealed at 800 °C. The chemical composition of the Er_2TiO_5 dielectric annealed various temperatures was analyzed by XPS. The Er 4*d* peak position at ~169.8 eV in Fig. 3 (a) indicates that Er is formed Er_2TiO_5 compound after annealing at 700 °C. In Fig. 3 (b) depicts the Ti 2*p* spectra, Ti 2*p* doublet (Ti $2p_{1/2}$ and Ti $2p_{3/2}$ at 465.6 and 459.7 eV, respectively) is shifted to higher binding energy compared to the TiO_2 reference position (Ti $2p_{1/2}$ and Ti $2p_{3/2}$ at 464.3 and 458.7 eV, respectively) [5]. This shift was attributed to Ti in Er_2TiO_5 structure. The O 1*s* signals in Fig.3 (c) further help in understanding layered structures. The low energy state centered at 531.2 eV is attributed to O in Er_2TiO_5. The median energy state, centered at 532 eV, is attributed interfacial O atoms in $ErSi_xO_y$. The high energy state, centered at 533 eV, is attributed to O in SiO_2 [6]. The O 1*s* peak intensity corresponding to Er_2TiO_5 suddenly increases at 800 °C. This suggests that the oxygen moving from the Er_2TiO_5 film was mostly consumed by the formation of SiO_2.

Fig. 4 illustrates the C-V curves for Er_2TiO_5 with different annealed temperature. Although the higher capacitance value in accumulation for as-deposited film is compared to sample annealed at 600 °C, this film exhibits the leakage of capacitance at ~-2V due the existence of some crystal defects. The decrease in flatband voltage and increase in capacitance value after PDA at 700 °C indicate that the oxide charges are removed in the Er_2TiO_5 matrix. The EOT of MOS device after annealing 700 °C is about 1.5 nm (k=22.8). It is found that the as-deposited film exhibits a large hysteresis voltage owing to more hole trapping in the metal oxide, as shown in Fig. 5. In addition, it could be observed that the dielectric annealed at 700 °C shows a very small hysteresis voltage (＜20 mV), indicative of the absence of interfacial electronics and/or mobile charge in the oxide. Fig. 6 demonstrates the J-V curves of Er_2TiO_5 with different annealed temperature. Although sample annealed at 800 °C exhibits a lower current density, the formation silicate and SiO_2 layer will occur during this annealing temperature. Fig. 7 illustrates conductance (G_m) and interface state density (D_{it}) with different annealing conditions. The sample annealed at 700 °C exhibited a lower conductance and D_{it} value, suggesting that the interface state and fixed charge are decreased after RTA treatment. Fig. 8 shows the charge trapping characteristics are examined by monitoring the changes in leakage current. The sample after annealing 700 °C has the smallest SILC and longest time to soft breakdown. As shown in Fig. 8 (b), after annealing at 700 °C, no significant changes in the leakage current were detected during the stress up to Vg=-1.5 V, indicating negligible charge trapping in the Er_2TiO_5 gate dielectric.

4. Conclusion

In this paper, a high-k Er_2TiO_5 gate dielectric film on Si has demonstrated that the sample after annealing at 700 °C in O_2 ambient shows a higher capacitance value, lower hysteresis voltage and interface trap density in C-V curves. This is due to the formation of an excellent amorphous structure and the reduction of low-k interfacial layer.

References

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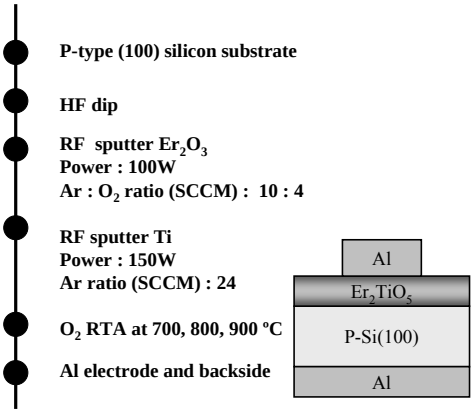

Fig. 1 The key process flow and MOS capacitor structure.

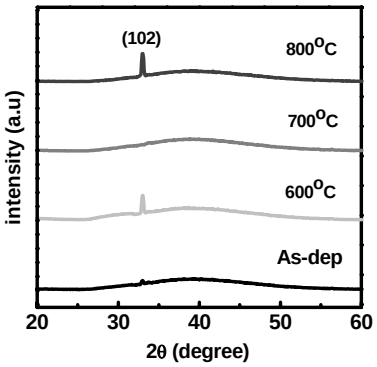

Fig. 2 XRD of Er_2TiO_5 films after annealing at various temperatures in O_2 ambient for 30 s

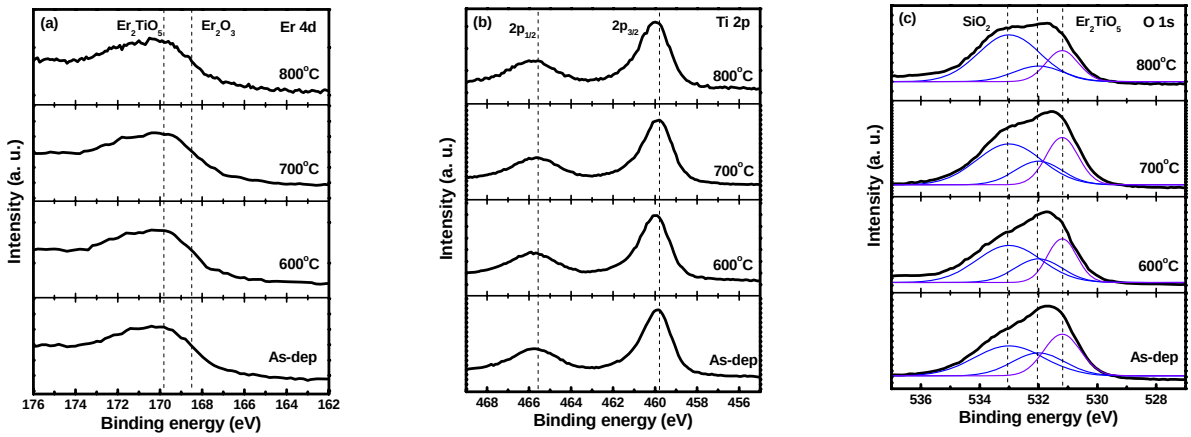

Fig. 3 XPS results of (a) Er 4*d*, (b) Ti 2*p* and (c) O 1*s* in Er_2TiO_5 film after annealing at various temperature

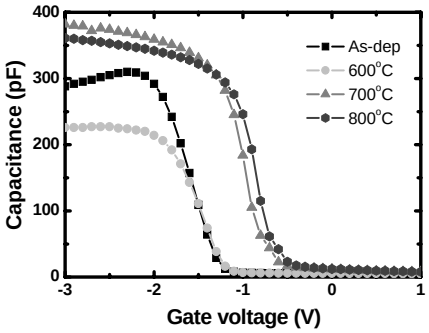

Fig. 4 The C-V curves for Er_2TiO_5 with different annealed temperature in O_2 ambient for 30s.

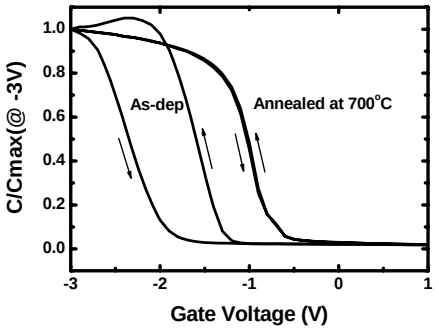

Fig. 5 The hysteresis phenomenon of MOS capacitors for as-deposition film and film after annealing at 700 °C

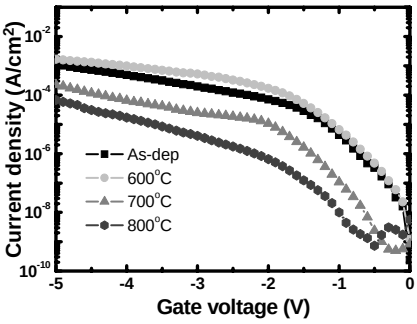

Fig. 6 The J-V curves for Er_2TiO_5 after different annealed temperature in O_2 ambient.

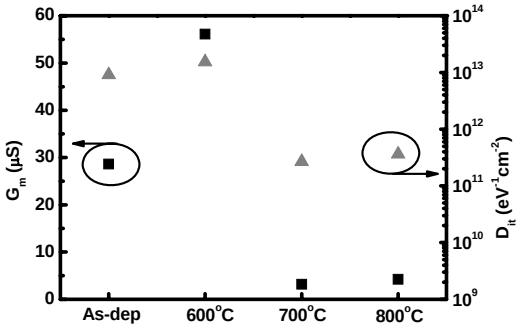

Fig. 7 The conductance (G_m) and interface state density (D_{it}) of Er_2TiO_5 gate films as a function of annealing temperature.

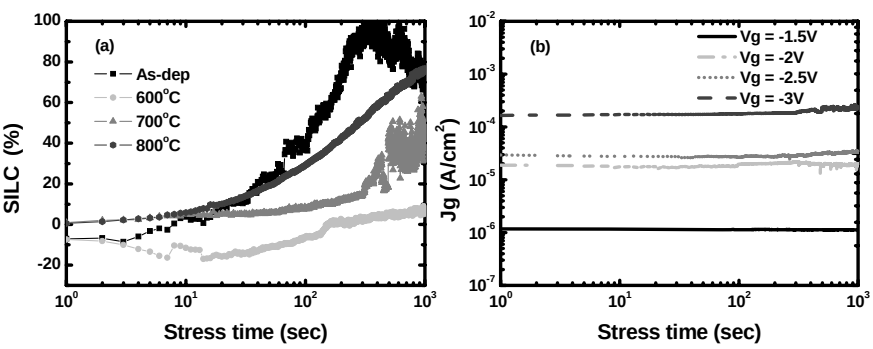

Fig. 8 (a) SILC [ΔJ/J(t=0), where ΔJ=J(t)-J(t=0)] (Vg=-3V) vs. stress time for MOS capacitors after annealing at different temperature (b) Charge trapping characteristics of Er_2TiO_5 gate film annealing at 700 °C during different constant voltage stresses.