In-Situ Fluorinated Low-Temperature Polycrystalline Silicon (LTPS) Thin-Film Transistors (TFT) with Low Trapping and Off Current by CF₄ Plasma

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1. Introduction

The polyoxide capacitors have attracted attention that the cause due to the possibility to realize the interpoly dielectric layer's memory [1] and thin film transistors (TFT) [2]. In most semiconductors of fluorine implant applications [3], it must have lower trapping rate and high dielectric breakdown field. In this work, in-situ fluorinated Low-Temperature Polycrystalline Silicon (LTPS) Thin Film Transistor (TFT) with low trapping and off current by CF_4 plasma was demonstrated.

2. Experiment

Aluminum/polyoxide/n⁺-polysilicon capacitors were fabricated in this study. P-type Si wafers were thermally oxidized to have an oxide of a thickness of 600 nm. Then, a polysilicon film (poly-1) of 300 nm was deposited at 625°C. It was implanted with phosphorous following activated for 30 sec in an N₂ ambient at 950°C to obtain a sheet resistance of 81~88 Ω/\Box . The polyoxide sample was treated under CF₄ plasma 30 sec and 1 min, respectively. The thickness of 50 nm of polyoxides were in-situ deposited by mixture SiH_4 and N_2O gas at 300 $^\circ\!C$ in the same chamber. An aluminum gate of a thickness of 300 nm was deposited on polyoxide films. After self-aligned defining aluminum gate and polyoxide patterned to form capacitors. The schematic polyoxide capacitors cross-section and detail process flow were shown in Fig. 1(a) and (b). For the device characterization, a polysilicon gate TFT was demonstrated also. The polyoxide capacitors and LTPS TFT performance was measured using a HP4156C.

3. Results and Discussion

Fluorinated Polyoxides

Figure 2(a) and (b) shows the J-E curves under both polarity for (a)- V_g and (b)+ V_g , respectively. The breakdown field was increased as increasing CF₄ plasma treatment. The leakage current was suppressed under the high electric field both for substrate (+ V_g) and gate (- V_g) injection. Figure 3(a) and (b) shows the gate voltage shifts of the - V_g and + V_g under constant current stresses for control and CF₄ plasma treatment samples. In Figure 3(a), the charge trapping properties of all samples had a hole trapping which has been attributed to produce the donor-like interface states at initial stress time, because of the PEOxide was kind of oxide of nitrogen contents (from N₂O gas mixture) and that the nitrogen piled up on top gate and polyoxide interface (SIMS plot not shown) [4]. In addition, It can be seen that the CF₄ plasma treatment of electron trapping rate of slope is slighter than control sample for both $-V_g$ and $+V_g$ constant current stress. Figure 4 shows the Weibull plots of charge-to-breakdown for control, pre-CF₄ 30 sec and 1 min polyoxide capacitors under 2μ A/cm² stress. The pre-CF₄ 1 min polyoxide has larger Q_{bd} and tight Q_{bd} distribution than control polyoxide sample. This improvement has been attributed to reduce electron trapping and strong Si-F bonding than Si-O on interface region. Figure 5 shows the fluorine ions effectively piled up at interface of secondary ion mass spectroscopy (SIMS) profile. The surface morphology of polyoxide was studied. Figure 6 and Fig. 7 shows the TEM and AFM image of surface of control, pre-CF₄ 30 sec and 1 min, respectively. In Fig. 6 and Fig. 7, the surface and root means Square (rms) variations were trifling on surface region.

Low-Temperature Polycrystalline Silicon Thin-Film Transistors

Figure 8 shows the transfer characteristics of TFTs for the control, pre-CF₄ 30 sec and 1 min. The off current values will decide the storage capacitors of loss charge degree in TFT array product application. It is known that the off current mechanisms were band-to-band tunneling (BTBT) and trap-assisted tunneling (TAT) near the drain edge. Therefore, how to passivate the trap-states effectively was very important. So we employ the CF₄ plasma to passivate the deep states and band tail states, and then to reduce the TAT mechanism. Consequently, it is seen that the off current was obvious improved following CF₄ plasma treatment time.

4. Conclusions

Polyoxide capacitors and LTPS TFT has be improved including the electric field of breakdown, trapping rate and Weibull distribution of charge-to-breakdown for polyoxide, consequently the OFF state current and breakdown voltage also be improved on LTPS TFT by CF_4 plasma treatment. The CF_4 plasma treatment could be applied to LTPS TFT manufacturing.

Acknowledgements

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References

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Fig. 1(a) The schematic cross-section for polyoxide capacitors, (b) process flow for polyoxide capacitors.

Fig. 2 The J-E characteristics of the control, pre-CF₄ 30 sec & 1 min treatment on N^+ -polysilicon films for the top gate applied with a (a) negative bias (b) positive bias.





Fig. 3 The curves of gate voltage shifts ($\triangle Vg$) versus stress time of the control, pre-CF₄ 30 sec & 1 min treatment on N⁺-polysilicon films for the top gate applied with a (a) negative gate constant current (under -0.2 μ A/cm²) stress (b) positive gate constant current (under 0.21 μ A/cm²) stress.

Fig. 4 The Weibull distribution Q_{bd} plots for the control, pre-CF₄ 30 sec & 1 min treatment on N⁺-polysilicon films for the top gate applied with a positive bias.



Fig. 5 SIMS profile analysis of silicon, oxygen, fluorine for pre-treatment CF_4 1 min.



Fig. 6 AFM images of N^+ -polysilicon surface of (a) control (b) pre-CF₄ 30 sec (c) pre-CF₄ 1 min samples with roughness root mean square (rms) of 3.9 nm, 3.8 nm and 4.3 nm, respectively.



Fig. 7 Cross-sectional TEM pictures of (a) control (b) pre-CF₄ 30 sec (c) pre-CF₄ 1 min samples, respectively.

Fig. 8 Transfer characteristics of the control, pre-CF₄ 30 sec & 1 min treatment of LTPS TFT.