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# Improvement of Electrical Characteristics for Novel Fluorine-Incorporated Poly-Si TFTs with TiN Gate Electrode and $Pr_2O_3$ Gate Dielectric

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## Introduction

In recent years low-temperature polycrystalline silicon thin-film transistors (poly-Si TFTs) have been widely used in active-matrix liquid crystal displays (AMLCDs) [1]. The major application of poly-Si TFTs in AMLCDs lies in integrating the peripheral driving ICs, and the pixel switching elements on the glass substrate to realize system-on-panel (SOP) purpose [2]. The peripheral driving ICs have the electrical characteristics requirement of low operation voltage, low threshold voltage, and high driving current, however conventional solid-phase crystallization (SPC) poly-Si TFT with $SiO_2$ as gate dielectric can not satisfy the needs. In order to address this issue, several high-κ gate dielectrics including $HfO_2$ and $LaAlO_3$ were proposed to increase the gate capacitance density for better gate controllability with keeping physical gate dielectric thickness [3],[4]. However, unfavorable gate-leakage was introduced from the crystalline high-κ material [5]. Recently, Praseodymium oxide ($Pr_2O_3$) becomes a promising high-κ material with high κ value, low gate-leakage, and superior thermal stability [6]. On the other hand, the detrimental GIDL current from the grain boundaries trap states was observed in the unhydrogenated poly-Si TFT [7]. Hence, fluorine ion implantation was utilized to passivate the trap states to improve the device performance [9],[10]. But it may not be suitable for glass application due to unfeasible large area implantation and high dopant activation annealing.

In this paper, an effective, low-cost, and process-compatible fluorine-based plasma treatment on poly-Si was proposed. We integrated TiN gate, high-κ $Pr_2O_3$ gate dielectric, and $CF_4$ plasma treatment with TFTs for the first time.

## 2. Experimental

The cross-sectional schematic diagram and the transmission electron microscopy (TEM) micrograph of the proposed metal gate, high-κ dielectric TFT are shown in Figs. 1, and 2. Briefly, the fabrication begins by depositing a 100-nm undoped amorphous silicon (α-Si) layer on a thermally oxidized Si wafers, followed by the SPC process. After the definition of active region, a $CF_4$ plasma was performed at 350 °C for 15 s with pressure of 200 mtorr and power of 10 W in PECVD chanber. Next, a 35-nm $Pr_2O_3$ film was deposited by e-gun evaporation system, followed by a furnace annealing at 600 °C for 30 min in $O_2$ ambient to improve the gate dielectric quality. A 300-nm TiN film was sequentially deposited, and then patterned to form gate electrode. Next, a self-aligned source/drain implantation, dopant activation, passivation oxide, contact hole, metal pads, and $N_2/H_2$ sintering were successively performed. For comparison, the control TFT without the $CF_4$ plasma treatment was prepared with the same process flow.

## 3. Results and Discussion

As shown in Fig. 3, the measured XPS spectra of the Pr 3d and O 1s core levels for $Pr_2O_3$ are in good agreement with previous data to well confirm the chemical composition of $Pr_2O_3$. Typical $I_{DS}$-$V_{GS}$ and $I_{DS}$-$V_{DS}$ of the integrated TiN gate and high-κ $Pr_2O_3$ TFTs with and without $CF_4$ plasma treatment are shown in Figs. 4, and 5; moreover, the key parameters were summarized in the table. 1. As $CF_4$ plasma is performed prior high-κ deposition, Vth decreased from 2.55 V to 2.28 V, S.S. decreased from 648 mV/dec to 575 mV/dec, $I_{ON}/I_{OFF}$ increased from $0.92 \times 10^7$ to$1.34 \times 10^7$, and trap density decreased from $5.23 \times 10^{12}$ $cm^{-2}$ to $2.89 \times 10^{12}$ $cm^{-2}$. This excellent performance is desirable for high-speed display IC's application resulted from the high gate capacitance density of $5.68 \times 10^{-7}$ $F/cm^2$ from C–V measurements, which gives a small equivalent-oxide thickness (EOT) of 6.07 nm. Furthermore, the effective κ value of $Pr_2O_3$ is extracted to be 22.5 from the physical thickness of $Pr_2O_3$ films, equal to 35nm, as shown in Fig. 2. Additionally, hot-carrier stress was applied at $V_D$ = $V_G$ = 4 V for 1000 s to examine the electrical reliability. The threshold voltage variations and the on-current degradation that resulted from the broken Si-Si and Si-H bonds during hot-carrier stress [11] are shown in Figs. 6, and 7. It was found that the $CF_4$ plasma treated TFTs have high immunity against the hot carrier stress as compared to control TFTs. Hence, the significant improvement in the electrical reliability can be attributed to the formation of stronger Si–F bonds in place of weaker Si–Si and Si–H bonds in the poly-Si.

## 4. Conclusion

A low cost, effective and process-compatible fluorine-incorporated technique is proposed. We have successfully combined TiN gate, $Pr_2O_3$ gate dielectric, and $CF_4$ plasma to fabricate high-performance poly-Si TFTs.

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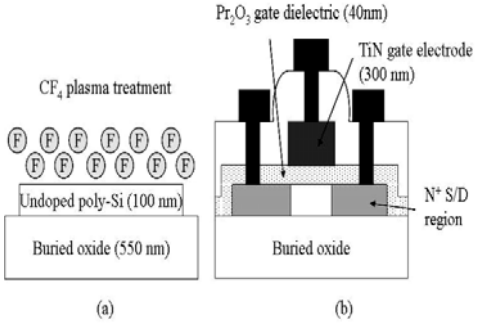


Fig. 1. Schematic diagram of the combined TiN gate and $Pr_2O_3$ gate dielectric TFT with $CF_4$ plasma treatment, (a) $CF_4$ plasma treatment on active region. Cross-sectional diagram of the proposed TFT structure.

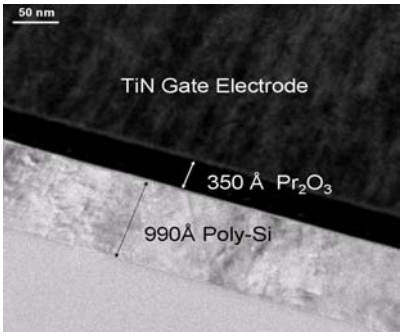


Fig. 2. Cross-sectional TEM image of the proposed high-κ $Pr_2O_3$ gate dielectric TFT structure.

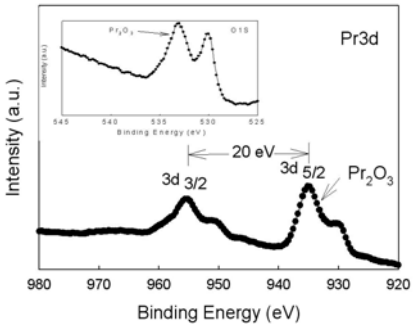


Fig. 3. Pr 3*d* photoelectron spectrum for $Pr_2O_3$.The inset also shows the O 1s photoelectron Spectrum which clearly indicates the presence of $Pr_2O_3$.

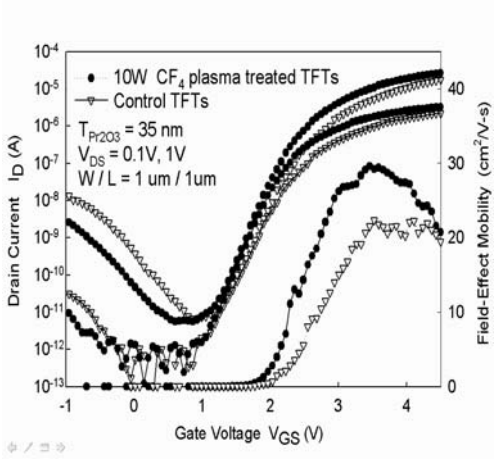


Fig. 4. Comparison of $I_D$–$V_G$ characteristics for control TFTs and $CF_4$ plasma treated TFTs (W/L = 1 μm / 1 μm).

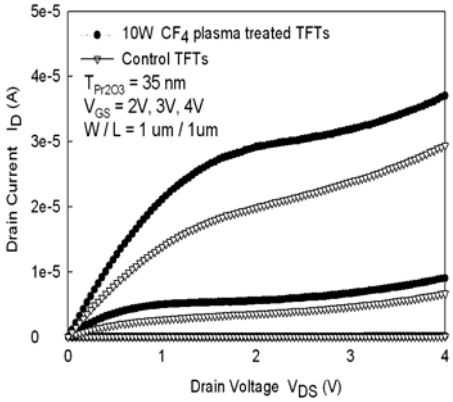


Fig. 5. Comparison of $I_D$–$V_D$ characteristics for control TFTs and $CF_4$ plasma treated TFTs (W/L = 1 μm / 1 μm).

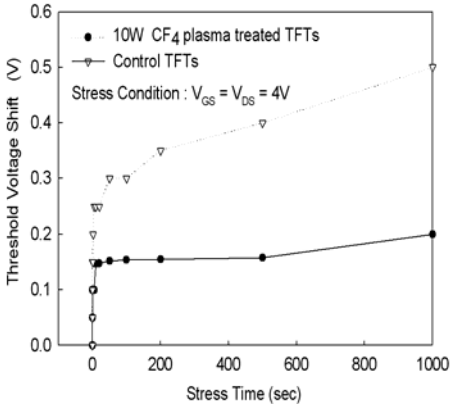


Fig. 6. Threshold voltage variation versus stress time for the control and $CF_4$ plasma treated TFTs.

Table 1. Key device characteristics for the $CF_4$ plasma treated TFTs and control TFTs

| Parameters | Control TFT | $CF_4$ plasma treated TFT |
|---|---|---|
| $V_{TH}$ (V) | 2.55 | 2.28 |
| S.S. (mV/dec) | 648 | 575 |
| $\mu_{FE}$ ($cm^2$/V-s) | 22.33 | 29.57 |
| $N_T$ ($10^{12}$ $cm^{-2}$) | 5.23 | 2.89 |
| $I_{ON}$ / $I_{OFF}$ ($10^7$) | 0.92 | 1.34 |

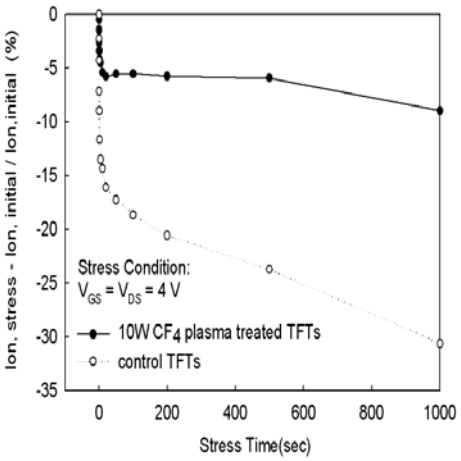


Fig. 7. On-current degradation versus stress time for the control and $CF_4$ plasma treated TFTs.


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