

P-10-12L

Reduction of Contact Resistance in Bottom Contact Pentacene-TFT by Employing Carrier Injection layer

Daisuke Kumaki¹, Tokiyoshi Umeda² and Shizuo Tokito^{1,2}

¹Department of Electronic Chemistry, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, 4259 Nagatsuta, Midori-ku, Yokohama 226-8502, Japan,

E-mail: kumaki.d.aa@m.titech.ac.jp

²NHK Science and Technical Research Laboratories, 1-10-11 Kinuta, Setagaya-ku, Tokyo 157-8510, Japan

1. Introduction

Organic thin-film transistors (OTFTs) are receiving considerable attention for use in the backplane of the active-matrix organic light emitting diode (AMOLED) displays fabricated on the flexible substrate[1]-[2]. High performances such as high on current, low operating voltage and rapid rise in subthreshold current are required for OTFT to drive the OLED display. In addition, these improvements of performances are especially needed in the bottom contact OTFT, because the photolithography patterning was used to realize higher resolution in the fabrication process of AMOLED display.

The reduction of contact resistance between source-drain (S-D) electrodes and organic semiconductor is important for the bottom contact OTFT to achieve the high performance[3]-[4]. In top contact OTFT, Chih-Wei Chu and co-worker improved the performance by employing bilayer S-D electrodes with metal oxide such as molybdenum oxide (MoO_x), vanadium oxide (VO_x) and tungsten oxide (WO_x)[5]. These metal oxides were well known materials as the carrier injection layer in OLED[6]. Additionally, it can be expected that the effect of the improvement in the bottom contact OTFT is larger than that of top contact OTFT.

We report on the reduction of contact resistance by employing S-D electrodes with MoO_x as the carrier injection layer in bottom contact pentacene-TFT. The contact resistance was estimated from the gated transfer length method (gated-TLM)[4] and compared with the conventional S-D electrodes (Cr/Au).

2. Fabrication Process

A schematic cross section of the bottom contact pentacene-TFT was shown in Figure 1. A highly doped silicon wafer with thermally grown SiO_2 (200 nm) was served as the common gate electrode and gate insulator. Two types S-D electrodes consisting of MoO_x /Au or Cr/Au were fabricated on the substrate. MoO_x layer was deposited by thermal evaporation from MoO_3 powder and then Au was formed on the MoO_x layer in the same vacuum chamber. The S-D electrodes were patterned by photolithography and lift-off process. Cr/Au electrode was deposited by e-beam evaporation and patterned by the same procedure. The channel length L and width W were 50 μm and 500 μm , respectively. After the lift-off process, the

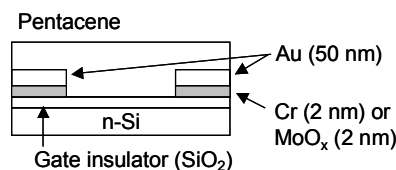


Fig. 1 Schematic cross section of the bottom contact pentacene-TFT.

substrate was immersed in HMDS solution for 8 h to improve the crystal growth of pentacene layer on the SiO_2 gate insulator. A 30-nm-thick pentacene, which was purified by the train sublimation twice, was formed on the substrate by thermal vapor deposition at room temperature (deposition rate 0.03 nm/s). The electrical characteristics were measured at room temperature by using an HP4140 source-meter system. Electrical characterizations were carried out in vacuum without exposure to air after the deposition of pentacene.

3. Improvement of TFT Performance

Figure 2 shows the plots of the drain current (I_D) (left) and square root of I_D (right) vs. gate voltage (V_G) at a drain voltage (V_D) of 50 V for the pentacene-TFT with the S-D electrodes of MoO_x (2 nm)/Au (50 nm) or Cr (2 nm)/Au (50 nm). MoO_x provided a high adhesiveness between the gate insulator and Au electrode and fine pattern. MoO_x carrier injection layer significantly improved the performance of the pentacene-TFT. Threshold voltage was reduced from 13 V to 0.2 V compared with the conventional S-D electrodes (Cr/Au). Drain current exceeded 10^{-5} A less than V_g of 20V, whereas the V_g of more than 40 V was needed in Cr/Au electrode for achieving the same current. The effect of improvement was especially large at the low operating voltage. The mobility in saturation regime was improved from 0.13 cm^2/Vs (Cr/Au) to 0.42 cm^2/Vs (MoO_x /Au) with the on/off ratio of 10^6 . MoO_x carrier injection layer showed the highest performance at the thickness of few nano meters (~ 2 nm), which was comparable to the effective channel thickness on the gate insulator in pentacene-TFT[7]. The improvement of TFT performance was clearly attributed to the reduction of contact resistance in the S-D electrode by employing the MoO_x injection layer.

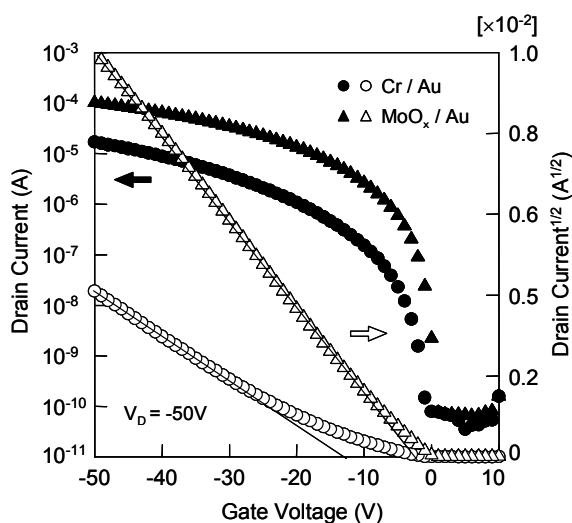


Fig. 2 I_D - V_G characteristics of pentacene TFTs with Cr/Au or MoO_x /Au S-D electrodes.

4. Evaluation of contact resistance

Figure 3 shows the highest molecular orbital (HOMO) level of the pentacene and work function of electrode materials. These values were estimated from the photoemission spectroscopic measurement in air (AC-3: Rikenkeiki). The Work functions of MoO_x and Cr were estimated to be 5.6 eV and 4.6 eV, respectively. The injection barrier height from MoO_x to pentacene was smaller than that from Cr. In addition, the vacuum level of the organic semiconductor is expected to shift downwards at the interface between organic semiconductor and metal[8]. Therefore the injection barrier height at the interface might be higher than the estimated value in Figure 3.

Figure 4 shows the gate voltage dependence of contact resistance in the bottom contact pentacene-TFTs with the S-D electrodes of MoO_x /Au or Cr/Au. Contact resistance was estimated from the gated-TLM[4]. Contact resistance of MoO_x /Au electrode was nearly one order of magnitude smaller than that of Cr/Au. This gate voltage dependence was consistent with the previous report[4]. In addition, contact resistance of Cr/Au rapidly increased with the gate voltage. The contact resistance was very high at the low gate voltage. The values of MoO_x /Au and Cr/Au were $2.4 \times 10^9 \Omega \mu\text{m}$ and $138 \times 10^9 \Omega \mu\text{m}$ at the V_G of 10V,

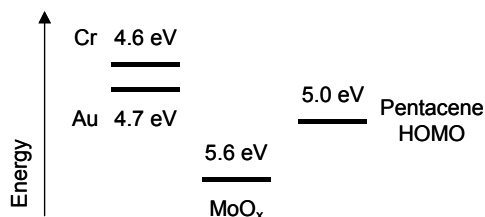


Fig. 3 Energy level diagram of pentacene and electrode materials.

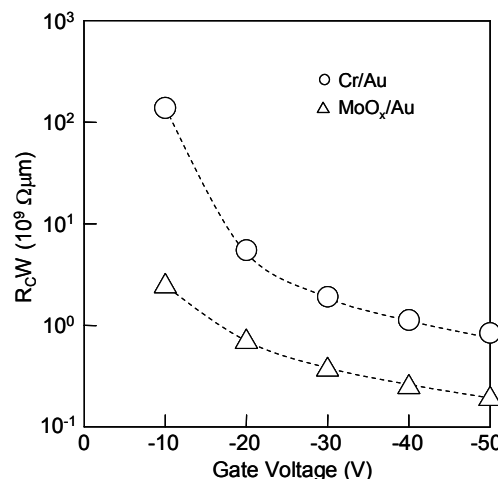


Fig. 4 Gate voltage dependence of contact resistance in pentacene TFTs with Cr/Au or MoO_x /Au S-D electrodes.

respectively. This result was consistent with the TFT performance shown in figure 2. MoO_x was effective in the reduction of contact resistance in the bottom contact OTFT.

5. Conclusions

We have fabricated the bottom contact pentacene-TFT with MoO_x carrier injection layer. By employing MoO_x carrier injection layer, TFT performance especially improved at the low operating voltage. threshold voltage was reduced from 13 V to 0.2 V and the mobility was improved from $0.13 \text{ cm}^2/\text{Vs}$ to $0.42 \text{ cm}^2/\text{Vs}$. MoO_x carrier injection layer significantly reduced contact resistance in bottom contact pentacene-TFT. Therefore MoO_x was effective in the reduction of contact resistance in bottom contact OTFT.

References

- [1] L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, *Appl. Phys. Lett.* **88** (2006) 083502.
- [2] M. Mizukami, N. Hirohata, T. Iseki, K. Ohtawara, T. Tada, S. Yagyu, T. Abe, T. Suzuki, Y. Fujisaki, Y. Inoue, S. Tokito, and T. Kurita, *IEEE Electron Device Lett.*, **27** (2006) 249.
- [3] N. Yoneya, M. Noda, N. Hirai, K. Nomoto, M. Wada, and J. Kasahara, *Appl. Phys. Lett.* **85** (2004) 4663.
- [4] D. J. Gundlach, L. Zhou, J. A. Nichols, and T. N. Jackson, *J. Appl. Phys.* **100** (2006) 024509.
- [5] C.-W. Chu, S.-H. Li, C.-W. Chen, V. Shrotriya, and Y. Yang, *Appl. Phys. Lett.* **87** (2005) 193508.
- [6] S. Tokito, K. Noda and Y. Taga, *J. Phys. D: Appl. Phys.* **29** (1996) 2750.
- [7] R. Ruiz, A. Papadimitratos, A. C. Mayer and G. G. Malliaras, *Adv. Mater.* **17** (2005) 1795.
- [8] H. Ishii, K. Sugiyama, E. Ito and K. Seki, *Adv. Mater.* **11** (1999) 605.