# Design of Reconfigurable Logic Circuits based on Single-Layer Magnetic-Tunnel-Junction Elements 

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## 1. Introduction

A magnetic-tunnel-junction (MTJ) has been used as a storage cell of magnetic random access memory (MRAM) [1]. Recently, a structure of triple-layer (TL) MTJ has been proposed to compute Boolean functions, which has three parallel input lines arranged vertically above the upper electrode (Fig. 1a) [2]-[4]. The magneto-logic using TL MTJs can replace CMOS logic both in a combinational logic and in a sequential logic. However, a TL MTJ requires more processing steps than a single-layer (SL) MTJ which is generally used as an MRAM cell (Fig. 1b). A magneto-logic using TL MTJs needs multiple driver circuits to precisely control the current through each layers which imposes significant burden on circuit density. In this paper, we propose a SL MTJ, as a magneto-logic element, along with a novel current driver circuit which is suitable to make reconfigurable logic circuits with simple construction. We present a reconfigurable 3-bit counter which can be programmed to operate as a gray counter (GC), an up counter (UC), or a down counter (DC).

## 2. The Reconfigurable Magneto-Logic 3-bit Counter

Basic concepts for a SL MTJ element with a current driver
There are parallel and anti-parallel magnetic states on MTJ, which are characterized by low $\left(\mathrm{R}_{\mathrm{L}}\right)$ and high $\left(\mathrm{R}_{\mathrm{H}}\right)$ resistance and are identified as logical 0 and 1 , respectively. The polarity of a fixed layer remains fixed, while the polarity of a free layer can be changed such that a positive current, +I , passing through layer 1 , makes the MTJ have $\mathrm{R}_{\mathrm{H}}$, and vice versa. The current driver shown in Fig. 2(a) determines the direction of the current flowing through layer 1. We design the current driver to control the combinatorial inputs, where the current through each of the constituent transistors is I. If all of the current driver inputs, $\alpha, \beta$, and $\gamma$, have logic ' 1 ', +3 I flows. If two of them have logic ' 1 ', +I flows through layer 1, and vice versa. Therefore, the Boolean expression for the MJT with current driver shown in Fig. 2(a) is given as

$$
\begin{equation*}
\text { OUT }=\alpha \cdot \beta+\beta \cdot \gamma+\gamma \cdot \alpha \tag{1}
\end{equation*}
$$

Inputs of $(0,1, \mathrm{~A}$, or Ab$),(0,1, \mathrm{~B}$, or Bb$)$, and $(0,1, \mathrm{C}$, or Cb ) can be applied to $\alpha, \beta$, and $\gamma$, respectively. Fig. 2(b) shows a simpler schematic of a SL MTJ with a current driver, where $\alpha, \beta$, and $\gamma$ correspond to $\mathrm{A}, \mathrm{B}$, and C , respectively. The Boolean expression becomes (A AND B)OR(B AND C)OR(C AND A) in that case.

A sense amplifier (S/A) is introduced in Fig. 3, to generate an output by comparing the resistance of the MTJ on the $\mathrm{V}_{+}$node with the one on the $\mathrm{V}_{\text {. }}$ node. The $\mathrm{V}_{\text {. }}$ node has an offset voltage (Vos) which satisfies eq. (2), thereby the S/A
output is high only when the voltage on $\mathrm{V}_{+}$node is higher than the voltage on V. node. As illustrated in Fig. 3, each of MTJs can be represented a single bit data having logic value at the 'out' node. The Boolean expression relevant to Fig. 3(a) is eq. (3) and the Boolean expression relevant to Fig. 3(b) is eq. (4) where MTJs are serially connected to each of the $\mathrm{V}_{+}$and the $\mathrm{V}^{-}$. node

$$
\begin{align*}
& \left.0<\mathrm{V}_{\text {OS }}<\mathrm{I}_{\text {SENSE }} \cdot \Delta \mathrm{R} \quad \text { (where } \quad \Delta \mathrm{R}=\mathrm{R}_{\mathrm{H}}-\mathrm{R}_{\mathrm{L}}\right)  \tag{2}\\
& \text { OUT }=\mathrm{W} \cdot \overline{\mathrm{Y}}  \tag{3}\\
& \text { OUT }=(\mathrm{W}+\mathrm{X}) \cdot \overline{\mathrm{Y}} \cdot \overline{\mathrm{Z}}+(\overline{\mathrm{Y}}+\overline{\mathrm{Z}}) \cdot \mathrm{W} \cdot \mathrm{X} \tag{4}
\end{align*}
$$

As shown in Fig. 4, a couple of SL MTJ can realize full logic functions according to the combinatorial inputs without any initialization procedure. (A AND B) is accomplished, where $\alpha, \beta$, and $\gamma$ in eq. (1) are $A, B$, and 0 , while (A XOR B) is accomplished, where (A OR B) is attached on $V_{+}$node and (AND B) is attached on $V_{-}$. node in eq. (3).

Embodiments of the magneto-logic 3-bit reconfigurable counter

In this section, we describe how a 3-bit reconfigurable counter works as a 3-bit GC, UC, and DC. Fig. 5 shows the circuit schematic which consists of eight MTJ elements for the counter. A, B and C are stored outputs of the previous operation, whereas $A_{\text {next }}, B_{\text {next }}$ and $C_{\text {next }}$ indicate the next states. A is the least significant bit. Inputs at $(\alpha, \beta, \gamma)$ for the next state of GC, UC, and DC are represented by default, italic, and bold type characters, respectively. The Boolean expressions for GC, UC, and DC are given as eq. (5), (6), and (7), respectively, each of which can be obtained from eq. (1), (2), (3), and (4) by applying appropriate inputs as shown in Fig. 5 .

$$
\begin{align*}
& \mathrm{A}_{\text {next }}=\overline{\mathrm{B} \oplus \mathrm{C}}, \quad \mathrm{~B}_{\text {next }}=\mathrm{A} \cdot \overline{\mathrm{C}}+\overline{\mathrm{A}} \cdot \mathrm{~B}, \quad \mathrm{C}_{\text {next }}=\mathrm{A} \cdot \mathrm{C}+\overline{\mathrm{A}} \cdot \mathrm{~B}  \tag{5}\\
& \mathrm{~A}_{\text {next }}=\overline{\mathrm{A}}, \quad \mathrm{~B}_{\text {next }}=\mathrm{A} \oplus \mathrm{~B}, \quad \mathrm{C}_{\text {next }}=(\mathrm{A} \cdot \mathrm{~B}) \oplus \mathrm{C}  \tag{6}\\
& \mathrm{~A}_{\text {next }}=\overline{\mathrm{A}}, \quad \mathrm{~B}_{\text {next }}=\overline{\mathrm{A} \oplus \mathrm{~B}}, \quad \mathrm{C}_{\text {next }}=(\overline{\mathrm{A}} \cdot \overline{\mathrm{~B}}) \oplus \mathrm{C} \tag{7}
\end{align*}
$$

The 3-bit counter shown in Fig. 5 can be easily reconfigured as GC, UC, or DC by switching input signals as indicated above. Furthermore, it can be shown that this structure can be expanded to implement arbitrary Boolean logic with three inputs by adding a MTJ to each of V+ and Vinputs of first two circuit blocks.

## Simulation Results using HSPICE Macro-Model

In our previous work, various characteristics of an MTJ have been modeled as a circuit macro-model for MRAM [5]. New macro-model for magneto-logic was made based on this model, such that the magneto-logic elements can be seamlessly integrated with CMOS logic circuits for

HSPICE simulation. We designed a test circuit for a 3-bit reconfigurable counter. Output waveform of the counter, simulated with HSPICE, is shown in Fig. 6. It can be observed that the output bits, $\mathrm{A}, \mathrm{B}$, and C keep changing one bit at a time for duration of GC, and increasing or decreasing by one at a time for duration of UC and DC , respectively.

## 3. Conclusions

The magneto-logic based on the MTJ has many potential advantages, such as non-volatility, increased speed, and low-power consumption. In this paper, we propose a SL MTJ with a current driver to build a reconfigurable counter, which has a simple construction and a flexible architecture. This novel scheme has ability to change its functionality on the same structure just by simple switching of the inputs. The proposed current driver lessens the area burden of multiple current drivers with the conventional TL MTJ. The proposed 3-bit reconfigurable counter can also be expanded into arbitrary Boolean logic three inputs. The 3-bit reconfigurable counter was designed with eight SL MTJs and its functionality was verified by HSPICE simulation using a macromodel of an MTJ.

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(a)

Fig. 1. Structure of the (a) conventional triple-layer magneto-logic element and (b) proposed single-layer magneto-logic element.


Fig. 6. HSPICE ${ }^{\text {TM }}$ simulation results of magneto-logic 3-bit reconfigurable counter.


Fig. 2. (a) Schematic of a SL MTJ with a current driver and (b) simpler schematic of the left one where inputs are $A, B$, and $C$.


Fig. 3. Schematic of S/A (a) for 2 MTJs and (b) for 4 MTJs.


Fig. 4. Magneto-logic gate (a) AND, (b) OR, (c) NOR, (d) NAND, (e) XOR, and (f) XNOR.


Fig. 5. Schematic of magneto-logic 3-bit reconfigurable counter

