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# Design of Vertical Nanowire FETs

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## 1. Introduction

Vertical wrap-gate nanowire field-effect transistors have been realized in various material systems including Si and InAs [1,2]. The transistors have demonstrated intriguing intrinsic transport properties including an extremely low subthreshold slope in Si interband tunnel transistors and a high electron mobility (μn about 10000 $cm^2$/Vs) in InAs transistors. The performance of vertical wrap-gate transistors with 100 nm gate length has further been simulated demonstrating advantageous intrinsic performance as a high performance logic device, including the gate delay, the energy-delay product, the subthreshold slope, and the $I_{on}/I_{off}$ ratio [3,4]. One major problem that has not been addressed so far is the design of realistic vertical transistors, in which the parasitic capacitances and resistances have been included. In this paper, we simulate the performance of a 3D InAs transistor structure, including the extended gate and drain contacts and their parasitics. It is shown that lateral scaling of the contacts allows transistor operation above 300 GHz at $V_{sd}$=0.5 Vfor $L_g$=50 nm.

## 2. Geometrical Layout and Simulation Method

The InAs nanowires used in these simulations have a quadratic cross-section with a side length of 50 nm. A 5-nm-thick $SiN_x$ layer ($\varepsilon_r$=7.5) is used as gate dielectric and a gate with 50 nm gate-length is employed. The gate-to-source separation is set to 100 nm, while the gate-to-drain separation is changed in the range of 200 to 500 nm. Under these geometrical conditions, simulations within the drift-and-diffusion formalism may still be valid as the wires are sufficiently thick to show negligible quantum confinement effects and the gate is sufficiently long to reduce the effects of ballistic transport. Besides, there are sufficient numbers of donor under the gate to reduce the influence of individual impurities.

Fig. 1 shows the layout of an experimental structure with a matrix of wires in the transistor and where the gate and drain contacts are connected to all the wires in parallel. The wires and the gate electrode are assumed to be embedded in a low-κ ($\varepsilon_r$=2.5) isolation layer. In typical experimental implementations, a nanowire spacing of 1 μm is used [2]. In order to facilitate the simulations, we have used a unit cell consisting of one quarter of a nanowire standing on a 0.5*x*0.5 $\mu m^2$ substrate that corresponds to the 1 μm matrix period. Besides, we have implemented a lateral scaling of the drain and gate electrodes using a cross-bar geometry as demonstrated in Fig 2. In this way, we reduce the overlay capacitance between the gate and drain.

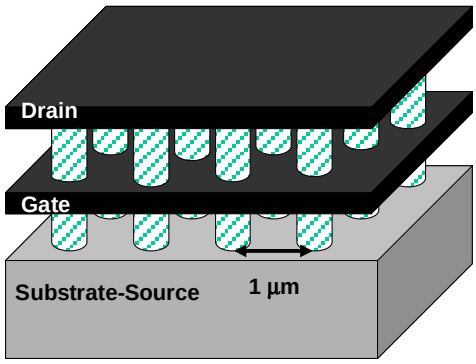


Fig. 1 Schematic layout of a vertical nanowire transistor.

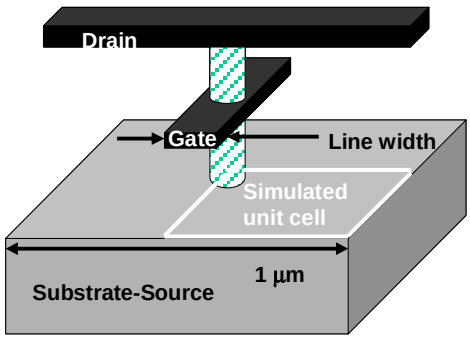


Fig. 2 Illustration of a single wire transistor with the gate and drain electrodes placed in a cross-bar geometry.

Given the geometrical conditions we simulate the performance within the drift-and-diffusion formalism using a mobility of 10000 $cm^2$/Vs and a saturated electron velocity of 3*x*$10^5$ m/s, values that have been deduced from fittings to experimental data [5]. Besides, the InAs affinity has been adjusted to the gate metal work junction to achieve a pinning 100 meV above the conduction band edge.

## 3. Simulation Results

In a first set of simulations we varied the line width of the gate and drain electrodes, using the same value for both. The gate-to-source spacing was set to 100 nm and the gate-to-drain spacing 200 nm, while the doping was 2x$10^{18}$ $cm^{-3}$ in the source and drain regions and 2x$10^{17}$ $cm^{-3}$ in the gate region. The low doped segment was aligned to the gate electrode. The simulated data for $C_{gg}$ and $C_{gd}$ (taken at $V_{sd}$=0.5V and $V_g$=0.2V) are shown in Fig. 3. As expected, the capacitances are dramatically reduced as the line width is decreased due to the reduced overlay capacitance between the contacts. As the line width is decreased from

1000 nm to 100 nm, $C_{gg}$ and $C_{gd}$ are reduced by 60 and 70 %, respectively. From the transfer characteristics, we also deduced the transconductance to be 520 μS per nanowire, which allowed us to calculate the cut-off frequency, ft, as $f_t=g_m/2\pi C_{gg}$. The scaling results in an increase in $f_t$ by more than a factor two, resulting in a $f_t$ of about 380 GHz. This data show that lateral scaling is effective to reduce the capacitances and that by patterning the electrodes with a line width of 200 nm or below, or alternatively by placing the nanowires with a spacing of 200 nm or less, a $f_t$ above 300 GHz may be realized for this transistor.

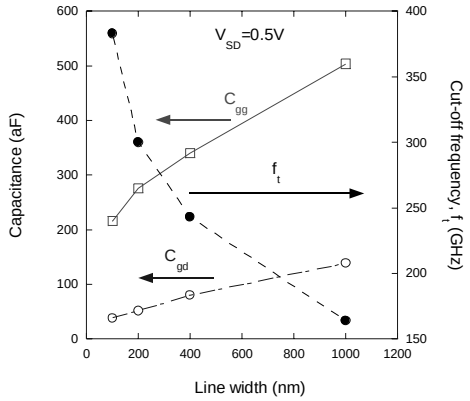


Fig. 3 Simulated capacitances and calculated $f_t$ for a single wire transistor with $2x10^{18}$ $cm^{-3}$ in the source and drain regions and $2x10^{17}$ $cm^{-3}$ in the gate region. $L_g$=50 nm.

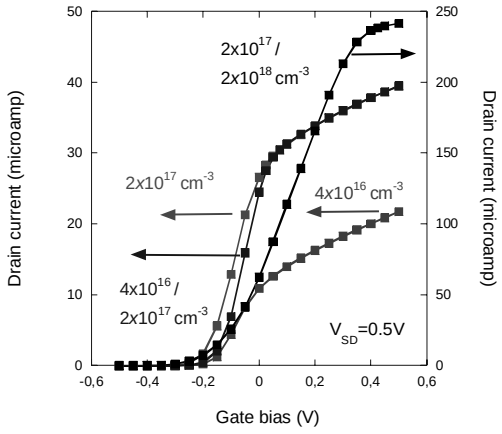


Fig. 4 Simulated transfer characteristics for devices with different doping levels.

Next, we studied the role of the doping in the nanowires for a line width of 200 nm. Fig. 4 shows simulated transfer characteristics at $V_{sd}$=0.5V, with doping levels experimentally found in InAs nanowires. In two cases, a lower doping has been introduced in the gate region to study the effect of the series resistance. All transistors show depletion mode operation with threshold voltages about -0.2 V. The data clearly shows that doping levels in the range of $10^{17}$-$10^{18}$ $cm^{-3}$ are required to enhance the transconductance and reduce the series resistance of the transistor. The deduced values for $g_m$, $C_{gg}$, $C_{gd}$ and $f_t$ are summarized in Table I, with a maximum simulated $f_t$ of 300 GHz. It should be noted that higher values for $g_m$ may be obtained with further increase in the doping level, but that this will cause a shift of the threshold voltage to more negative values.

Table I Simulated properties of nanowire transistors with various doping levels. The source-to-drain spacing is set to 100 nm and the gate-to-drain spacing to 200 nm. The lightly doped segment is introduced directly under the gate. $L_g$=50 nm.

| Doping level ($cm^{-3}$) | $g_m$ (μS) | $C_{gg}$ (aF) | $C_{gd}$ (aF) | $f_t$ (GHz) |
|---|---|---|---|---|
| $4x10^{16}$ | 89.2 | 292 | 53.2 | 48 |
| $4x10^{16}/2x10^{17}$ | 168 | 284 | 53.6 | 94 |
| $2x10^{17}$ | 150 | 288 | 53.6 | 83 |
| $2x10^{17}/2x10^{18}$ | 520 | 272 | 51.6 | 305 |

Finally, we also changed the gate-to-drain separation to evaluate the influence on the capacitances, Table II. The data show that a 15% decrease in $C_{gd}$ may be achieved by increasing the separation from 200 to 500 nm without any dramatic change in $g_m$ or $C_{gg}$. This reduction in the feed-back capacitance may be beneficial in analogue applications. A further reduction in $C_{gg}$ may also be achieved via patterning of the source electrode.

Table II Simulated properties of nanowire transistors with various gate-to-drain spacing. The source-to-drain spacing is set to 100 nm and the doping $2x10^{18}$ $cm^{-3}$ with a low doped segment ($2x10^{17}$ $cm^{-3}$) introduced directly under the gate. $L_g$=50 nm.

| Gate-to-drain spacing (nm) | $g_m$ (μS) | $C_{gg}$ (aF) | $C_{gd}$ (aF) | $f_t$ (GHz) |
|---|---|---|---|---|
| 200 | 520 | 275 | 51.6 | 301 |
| 300 | 520 | 276 | 47.6 | 300 |
| 500 | 520 | 285 | 44.8 | 290 |

## 4. Summary

We have in summary studied the performance of a vertical InAs nanowire transistor as a function of the geometry and the doping levels. It is found that a $f_t$ above 300 GHz may be achieved at $V_{sd}$=0.5 V for a 50 nm gate length when the electrode line width is scaled to 200 nm or below.


## Acknowledgements

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