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Simulation and fabrication of embedded capacitors in the multilayer printed circuit board

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1. Introduction

SOP(System on a Package) provides an exciting area for evaluating the usefulness of embedded electronics component because the application is somewhat more focused than that of more generalized consumer electronics. Specially, passive components become of increasing interest because the number of passive components is steadily growing as the electronics industry is progressing toward higher functionality. Integral embedded passive technology may satisfy such demands. The main advantages of embedded passive components include: (1) no separate interconnects to the substrate, (2) improved electrical performance, (3) lower cost and (4) ease of processing. Among passive components, special interest is given to capacitors, because they are used in large numbers for various functions, such as decoupling, bypassing, filtering, and timing capacitors

2. Experimental

In this experiment, for all embedded capacitors, the general build-up of the PCB is the same. The substrate consists of eight layers. The cross-section is non-symmetrical. All metal layers are from 12 μm to 28 μm thick. For reducing the size of the embedded capacitors, the used high dielectric composite material is comprised of barium titanate($BaTiO_3$) powder and epoxy resin. It has relative dielectric constant of 30 and loss tangent(δ) of 0.02. The fabricated embedded MIM capacitors located on 2nd layer have the cured thickness of 16 μm. The GSG (Ground-Signal-Ground) test pads are finally formed and via-interconnected with the previously formed input / output ports and ground plane on the 1st layer. All through holes via of embedded capacitors are connected to all cupper plates. The fabricated PCB embedded capacitors have been measured and characterized by using an HP 8510B network analyzer and PICOPROBE coplanar ground-signal-ground (GSG) probes with 250μm pitch size. The measured frequencies are ranged from 0.1 GHz to 10 GHz for mobile and wireless system applications.

3. Results and discussions

Fig. 1 a) and b) display the cross section and top images of embedded capacitors in the multilayered PCB. Figure c) and d) show real views of embedded capacitors and ground-signal-ground electrodes on the multilayered PCB. Fig. 2 exhibits frequency dependent impedance behavior of simulated embedded capacitors and fabricated embedded capacitors according the frequency range from 100 MHz to 10 GHz. Embedded capacitors were designed to increased capacitance value and decreased inductance and resistance values. Fig. 3 displays frequency dependent capacitance behavior of simulated and fabricated embedded capacitors. These embedded capacitors have dielectric constant of 30, capacitance values of 10, 5, and 2 pF. The capacitance value can be extracted from the impedance value employing the equation (1).

$$C_S = -\frac{1}{\omega(\mathrm{Im}(Z))} = -\frac{1+\omega^2 C^2 R_p^2}{\omega^2 L - \omega^2 C R_p^2 + \omega^4 C^2 R_p^2 L} \quad \text{- (1)}$$

Simulated capacitance values of embedded capacitors were well matched with the capacitance values of fabricated embedded capacitors. Fig. 4 exhibits the frequency dependent quality factor of simulated and fabricated embedded capacitors in the multilayered printed circuit board. As shown in the figure, quality factor of 20 was simulated and measured at the 2 GHz range employing 10 pF embedded capacitors. In the case of 10 pF embedded capacitor, the simulated and measured quality factor were almost similar in the whole frequency range. By decreasing the capacitance from 10 to 2 pF, insertion loss plays a role to increase loss tangent compared with large capacitance. Therefore quality factor of measured 2, and 5 pF embedded capacitors were deviated from the simulated values. Fig. 5 displays the temperature dependent dielectric permittivity and loss tangent of 2, 5, and 10 pF embedded capacitors made on the 8-layerd PCB. 2, 5, and 10 pF of fabricated embedded capacitors have 5.9, 7.3, and 8.9 % variance of capacitance as the temperature changed from the 20 °C to 130 ℃, respectively. All specimens have relative small loss tangent less than 0.0266 at all temperature range.

4. Conclusions

In this research, we have simulated and fabricated embedded capacitors in the multilayer printed circuit board employing high dielectric materials. Frequency dependent impedance of simulated and fabricated embedded capacitors was investigated. Fabricated embedded capacitors have lower self resonance frequency values than that of the simulated embedded capacitors due to the increased parasitic inductance values. Frequency dependent capacitance values of fabricated embedded capacitors were well matched with that of simulated embedded capacitors from the 100 MHz to 10 GHz range. Quality factor of 20 was observed and simulated at 2 GHz range in the 10 pF embedded capacitors. Temperature dependent capacitance of fabricated embedded capacitors was performed. 5.9 % of capacitance variance was measured in the 2 pF of fabricated embedded capacitors from the 20 to 120 °C.

References

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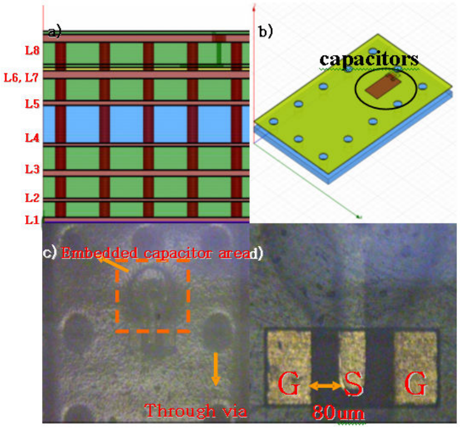

Fig. 1 a) cross-section of 8 layered PCB, b) oblique view of embedded capacitors on the 8 layered PCB, c) top view of Embedded capacitor area and, d) GSG (Ground-Signal-Ground) test pads

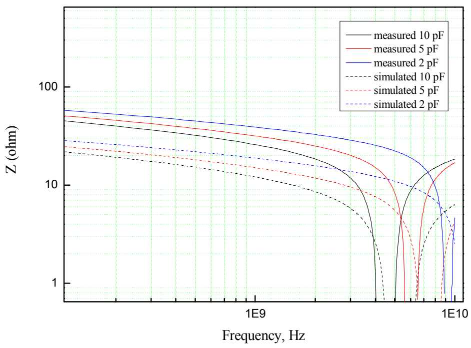

Fig. 2 Impedance value of simulated and fabricated embedded capacitors as a function of frequency.

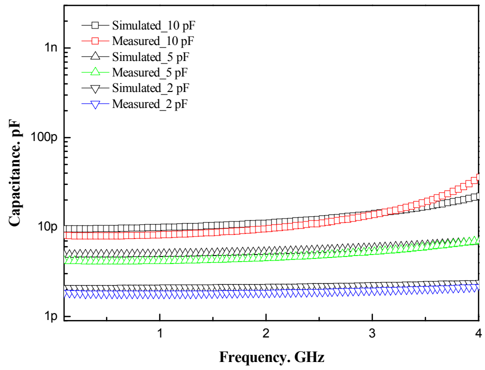

Fig. 3 Frequency dependent capacitances of simulated and fabricated embedded capacitors.

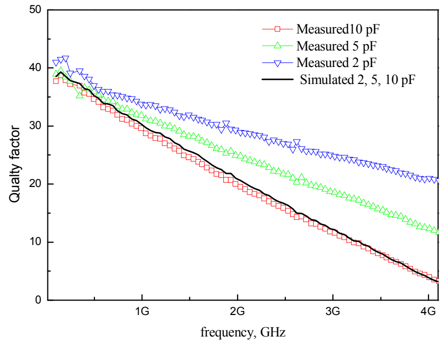

Fig. 4 Frequency dependent quality factors of simulated and fabricated embedded capacitors

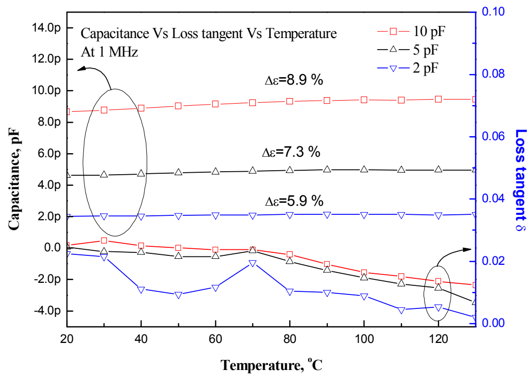

Fig. 5 temperature dependent capacitance and loss tangent of fabricated embedded capacitors.