

# Non-destructive extraction of width bias variations for deep sub-micron interconnect lines

P-2-11

Mao-Chyuan Tang, Meng-Feng Wang, Tim Cheng, David Chen, C S Yeh and S C Chien

Central R &amp; D Division, United Microelectronics Corp. Tainan, Taiwan

Tel: 886-6-5054888 ext 12287, Fax: 886-6-5050968, E-mail: mao\_chyuan\_tang@umc.com

## Abstracts

In this paper, we propose a model of the width bias variation effect caused from non-ideal optical proximity correction (OPC) in deep sub-micron interconnect lines. By our electrical-only and non-destructive methodology, an accurate table of width bias or WEE (wire edge enlargement), which is necessary for back-end-of-line (BEOL) design on advanced deep sub-micron technology, can be fully extracted with error less than 5%.

## 1. Introductions

For deep sub-micron ULSI technology, as the size of interconnects (width and spacing) is scaling, because of non-linear distortion by optical diffraction, the real size on silicon is not always equal to the intended drawn size by the BEOL designers. In order to reduce the non-linear distortion depending on pitch (width plus spacing) and pattern density, we usually apply OPC to increase the manufacturing yield and reliability. But unfortunately, non-linear distortion in real world situations will not disappear even after application of OPC [1]. This is called the width bias variation effect, which will be more severe as the pitch scales down to the minimum rules.

Previously the width bias variation effect was not considered as the variation is little compared to the width or spacing. When using the advanced deep sub-micron technology, inherent error up to 30% may be occurred at minimum rules if this effect was not taken into account. Traditionally it is often to use time-wasting method such as simulation tools to fit capacitance curves [2][3], or other destructive methods like transmission electron microscopy (TEM) or scanning electron microscopy (SEM) to extract the metal width and thickness. In this paper, we propose a methodology with the advantages of non-destructive and time-saving to extract the width bias with high accuracy less than 5%.

## 2. Experiments

Figure 1 shows the test-key structure where there is a signal line with two adjacent grounding lines on two sides between two floating plates. We choose M1 (metal 1), M3 and M8 of deep sub-micron process responsible for different BEOL processes for the experiment. The electrical measurements of metal line capacitance and resistance are based on the charge-based capacitance measurement (CBCM) method [4] and Kelvin structure [5], respectively, with high resolutions. For CBCM measurement, putting the same lead lines on reference side as those from driving transistor to the signal line on the experiment side, pure capacitances responsible for the signal lines can be derived by subtracting these common parasitic capacitances.

## 3. Results and Discussions

Fig. 2 shows the signal line structure and the influence of resistance in this effect on M1 interconnect wires. The cross section of metal is assumed to be rectangular. Because the resistance of the barrier is much larger than for copper, the reciprocal of the metal line resistance can be shown as follows:

$$\frac{1}{R} = \frac{(T_M - T_B) \times (w + \Delta w - 2\Delta)}{\rho \times L} = \frac{T_M - T_B}{\rho \times L} \times w + \frac{T_M - T_B}{\rho \times L} \times (\Delta w - 2\Delta) \quad (1)$$

where  $\rho$  and  $L$  are the resistivity and length of copper respectively, and the other parameters are shown in inset of Fig. 2. Please note that 4X~1X are referred to the multiples of minimum rules in width or spacing for every metal layer. From (1), the relationship between  $1/R$  and width is linear for fixed  $\Delta w$  and  $T_M$ . This linear relationship is very clear for widths of 4X to 2X for all spacings. However, the deviation from the linear trend at 1X width originates from the different  $\Delta w$ . The effect is less serious for M3 and M8 than for M1, as shown in Fig. 3 and 4 respectively, because the ratio of  $\Delta w$  to width or spacing is small enough to neglect the variation between the real and drawn width. In addition, the width biases of spacings of 2X to 4X should be the same because these three lines overlap. These three overlapped lines are different from that of 1X spacing due to the increased ratio of width bias to spacing. From (1),  $\Delta w$  at large width, denoted by  $\Delta w_1$ , can be derived as follows:

$$\Delta w_1 = \frac{\text{intercept}}{\text{slope}} + 2\Delta \quad (2)$$

where the intercept is  $\frac{T_M - T_B}{\rho \times L} \times (\Delta w - 2\Delta)$  and the slope is  $\frac{T_M - T_B}{\rho \times L}$ . The advantage of this equation is that it would not be influenced by erosion, dishing, or variation in resistivity. Due to the same slope in Fig. 2 for widths from 4X to 2X at any spacing for M1, the value of  $(T_M - T_B)/\rho L$  is almost the same. This means that if the changes in resistivity  $\rho$  are small, metal thickness  $T_M$  responsible for dishing or erosion effect is unchanged for fixed  $T_B$ . The same is true for M3 and M8.

The total capacitance  $C_T$  as shown in (3) is composed of the area capacitance  $C_a$  (proportional to real width), the coupling capacitance  $C_c$  (inversely proportional to real spacing), and the fringing capacitance  $C_f$  (a weak function of real spacing).

$$C_T = C_a + C_c + C_f = \left( \frac{\epsilon_d T}{t_T} + \frac{\epsilon_{dB}}{t_B} \right) \times (w + \Delta w) + \frac{\epsilon_s \times T_M}{s - \Delta w} + C_f \quad (3)$$

where  $\epsilon_d T$  ( $\epsilon_{dB}$ ) and  $t_T$  ( $t_B$ ) refer to the equivalent permittivity and the thickness of the dielectric between the metal line and the top (bottom) plate, respectively.  $\epsilon_s$  is the equivalent permittivity of the spacing. Fig. 5 shows the linear relationship between  $C_T$  and signal line width for widths of 4X to 2X for all spacings of M1. The linear trend of  $C_T$  with width implies the spacings between two metal lines are equal (it means equal width bias  $\Delta w$ ) so that  $C_c$  is the same for all these cases. If the width biases at each width in the same spacing are not equal,  $C_c$  would also be changed as shown in (3) and  $C_T$  would not be linear with width. There are also deviations from the linear trend for widths of 2X to 1X. This deviation shows that  $C_c$  is different for these two cases because of the change in  $\Delta w$ . Fig. 6 shows the cases for M3. Because  $C_c$  at some width is inversely proportional to spacing, so

$$\frac{C_{C3}}{C_{C2}} = \frac{S_{2(\text{real})}}{S_{3(\text{real})}} = \frac{S_{d(\text{drawn})} - \Delta w_2}{S_{d(\text{drawn})} - \Delta w_1} \quad (4)$$

where  $C_{C2}$  is the coupling capacitance at point 2 of Fig. 5 and can be extracted from the test-key structure shown in Fig. 7.  $C_{C1}$  can be derived as follows:

$$\Delta C_c = \Delta C_T - C'_a(w_2 - w_1) = \Delta C_T - C'_a(\Delta w_2 - \Delta w_1) \quad (5)$$

where  $C'_a = \Delta C_a / \Delta w = \Delta C_T / \Delta w$ . The width bias at small width, denoted by  $\Delta w_2$  which differs from that at large width, can be extracted from (4) and (5).

Fig. 8 compares experimental data with the results of the Raphael simulation of the extracted width bias table for M1, and Fig. 9 shows the comparison for M3. The percentage errors are below 5% without any tuning for M1 as shown in Fig. 10. Because the influence on M8 is small, the differences between considering and not considering width bias effect are very small.

#### 4. Conclusions

The width bias variation effect is most significant especially when width and spacing reach the minimum rules at lower metal layer. We have successfully developed an electrical-only and non-destructive methodology, which could also be applied to future advanced deep sub-micron technology, to extract width bias by using specific test keys for capacitance and resistance.

#### References

- [1]. M. Aoyagi, et. al, *IEEE Applied Superconductivity*, pp381-384, 2001.
- [2]. D. Sylvester, et. al, *Proceeding of IEEE*, pp634-664, 2001.
- [3]. X. Li, et. al, *IEEE TED*, pp2272-2279, 2005.
- [4]. K. Harazaki, et. al, *International Microprocesses and Nanotechnology Conference*, pp11-13, 2000.
- [5]. D. Sylvester, et. al, *IEEE J. SSC*, pp449-453, 1998.

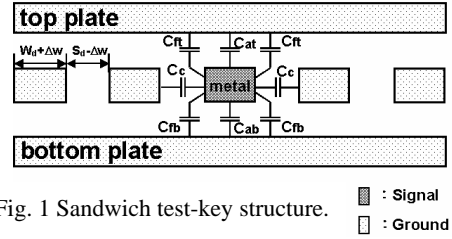


Fig. 1 Sandwich test-key structure.

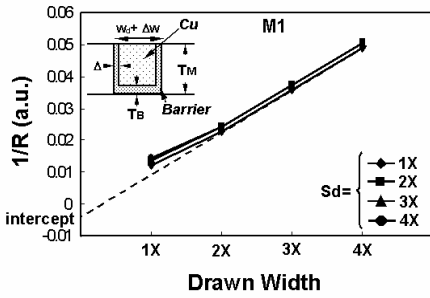


Fig.2 Resistive relationship versus drawn width for M1. Inset is the cross section of the signal line. 1X to 4X for width and spacing are referred to the multiples of M1 minimum rules in width and spacing, respectively.

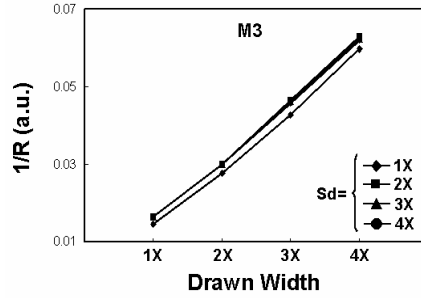


Fig.3 Resistive relationship versus drawn width for M3. 1X to 4X for width and spacing are referred to the multiples of M3 minimum rules in width and spacing, respectively.

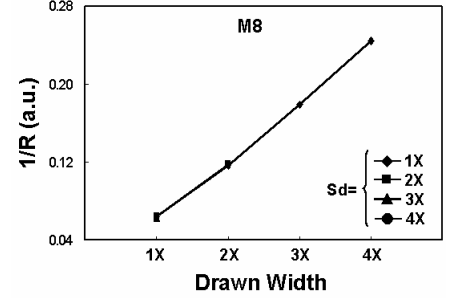


Fig.4 Resistive relationship versus drawn width for M8. 1X to 4X for width and spacing are referred to the multiples of M8 minimum rules in width and spacing, respectively. Less width bias variation is apparent.

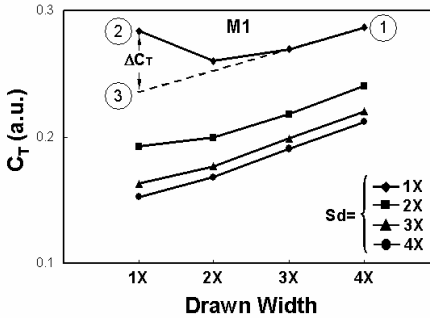


Fig.5 Capacitive relationship versus drawn width for M1. The width bias  $\Delta w$  at point 3 is the same with that at point 1. 1X to 4X for width and spacing are referred to the multiples of M1 minimum rules in width and spacing, respectively.

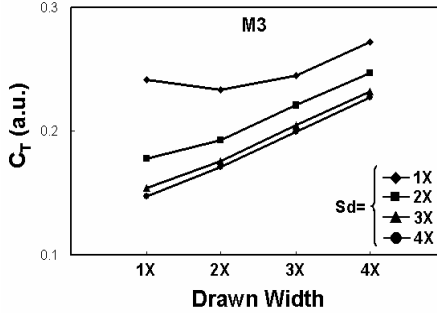


Fig.6 Capacitive relationship versus drawn width for M3. 1X to 4X for width and spacing are referred to the multiples of M3 minimum rules in width and spacing, respectively.

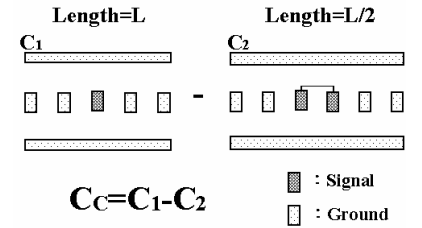


Fig. 7 Test-key structure of  $C_c$  extraction.

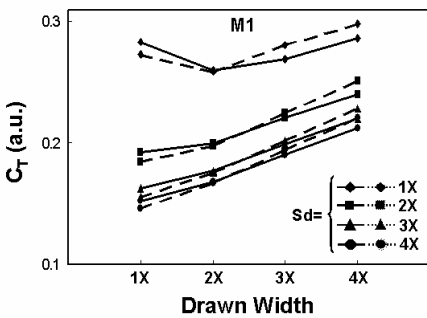


Fig.8 Comparisons of capacitance of experimental data (solid lines) and Raphael simulation (dashed lines) of our extracted width bias table for M1. 1X to 4X for width and spacing are referred to the multiples of M1 minimum rules in width and spacing, respectively.

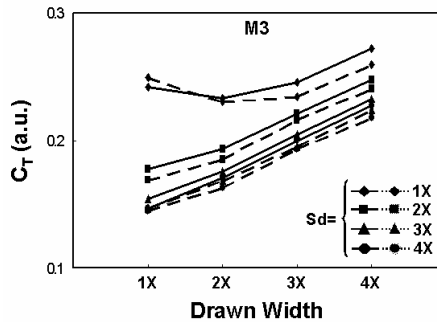


Fig.9 Comparisons of capacitance of experimental data (solid lines) and Raphael simulation (dashed lines) of our extracted width bias table for M3. 1X to 4X for width and spacing are referred to the multiples of M3 minimum rules in width and spacing, respectively.

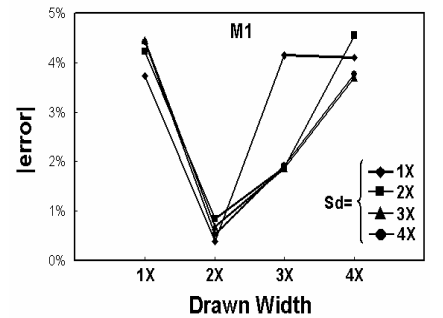


Fig.10 Errors of Raphael simulation of our extracted width bias table compared with experimental data for M1 layer. Errors are below 5%. 1X to 4X for width and spacing are referred to the multiples of M1 minimum rules in width and spacing, respectively.