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Void Free Room Temperature Silicon Direct Bonding by Sequential Plasma Activated Process

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1. Introduction

Silicon direct wafer bonding is developing as a promising approach for manufacturing silicon-on-insulator (SOI), MEMS and 3D integration of semiconductors [1]. Generally conventional silicon bonding requires annealing temperature above 700~1000ºC to achieve sufficient bonding strength. But this high temperature will take some problems, e.g. alignment difficulty, gas formation in the cavity and damage of temperature-sensitive devices. To realize annealing temperature as low as possible, many efforts have been done to activate the wafer surfaces prior to bonding, such as using O_2 (or Ar, N_2) plasma [2], O_2 plasma involving wet chemical cleaning [3]. However, the bonding strength is usually weak at room temperature and low temperature annealing (200~400ºC) is still needed. Moreover, a large number of voids are generated in the annealing process [4]. These annealing voids are quite harmful for subsequent process and device reliability. Therefore, room temperature wafer bonding without subsequent annealing voids is highly desirable.

Sequential plasma activated bonding has been developed recently. By this method, very strong bonding strength of Si/Si enables to be achieved at room temperature. Unfortunately, many annealing voids are also generated in previous study [5]. In order to overcome this problem, the sequential plasma activated bonding process is optimized in this paper. Strong bonding strength of Si/Si is demonstrated at room temperature, as well as avoiding subsequent annealing voids even if the bonded wafer pairs are heated.

2. Experimental

8-inch, 725 μm thick silicon wafers are used. All the wafers are p-type, (100) oriented, one side polished, Czochralsky (CZ) grown bare wafers. The wafers were load into the plasma chamber, and then the wafer surfaces pretreated by O_2 reactive ion etching (RIE) plasma at 30 Pa and followed N_2 radicals at 30 Pa at room temperature (RT). After the pretreatment, the two wafers were taken out of the chamber and brought into contact in ambient air under hand-applied pressure. And then the pre-bonded wafers were cold rolled under 75 kgf to remove unbonded regions. The bonded wafer samples were prepared by the process A, B, C, D or E as listed in Table I.

The bonding energy of Si/Si was calculated by inserting 100 μm thick razor blades, namely crack opening method. Some bonded wafer samples were loaded into the oven (P100 KFC Corp.) to be annealed. Annealing processes in this paper do not aim to improve the bonding strength, but to investigate void formation at the bonded interfaces. The voids were detected through infrared (IR) camera and UV-visible spectrometer (Perkin-Elmer Lambda 900). The cross section of bonded interfaces was etched by KOH solution to inspect the small voids.

Table I Different wafer bonding process studied in this work

No.	Process		
	O_2 RIE plasma	N_2 radicals	Storage at RT in air after contact and rolling
A	10 s	60 s	24 h
B	60 s	60 s	24 h
C	60 s	60 s	0 h
D	10 s	60 s	100 days
E	60 s	60 s	100 days

3. Results and Discussion

Figure 1 shows the bonding energies of samples A and B. Bonding energies are so high that we cannot insert the razor blades without breaking the bonded wafers in most cases. Furthermore, the sample A was diced into 10×10 mm^2 pieces. Ten pieces of small samples were taken randomly for the pulling tensile test. And all of them were fractured at the glue (the maximum force was 1470 N, equivalent to 14.7 MPa). These results imply that the bonding strength of Si/Si performed by these sequential plasma processes is very strong at room temperature, close to the bulk-fracture of silicon (~2500 mJ/m^2).

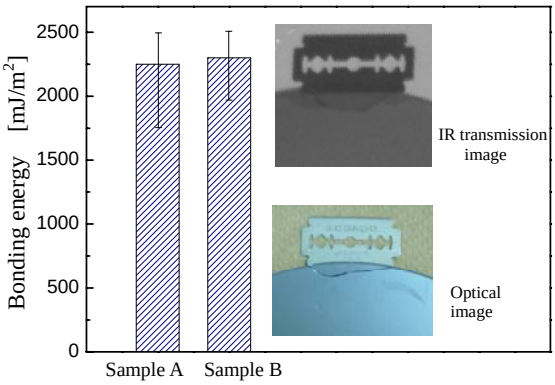


Fig. 1 Bonding energies of sample A (pretreated by O_2 RIE 10 s + N_2 radicals 60 s) and B (pretreated by O_2 RIE 60 s + N_2 radicals 60 s), the sample A was broken by inserting razor blade (right images) as an example

Some samples of A, B and C were annealed at 200, 300, 400, 500, 600, 700 and 800ºC for 7 hours in air ambient respectively. The plasma pretreatments of the sample B and C are same, but the sample C is annealed immediately without storage at RT after the bonding. Many voids are observed at 800ºC for the samples B and C [Fig. 3(b) and (c)]; whereas void density of the sample A is much lower (only 1% void density). Moreover, voids become to decrease from 700 to 800ºC. And the remained voids at 800ºC are mainly caused by initial particulates in our class 10 K clean room [Fig. 3(a)]. Therefore, voids could be minimized in a better clean room environment.

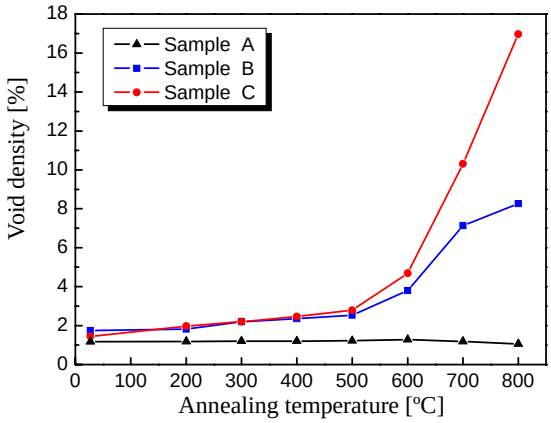
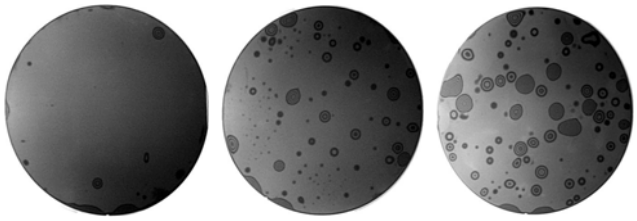


Fig. 2 Evolution of void densities as a function of annealing temperatures for the bonded wafers



(a) (b) (c)

Fig. 3 IR transmission images of samples A (a), B (b) and C (c) after annealing at 800ºC for 7 h, respectively

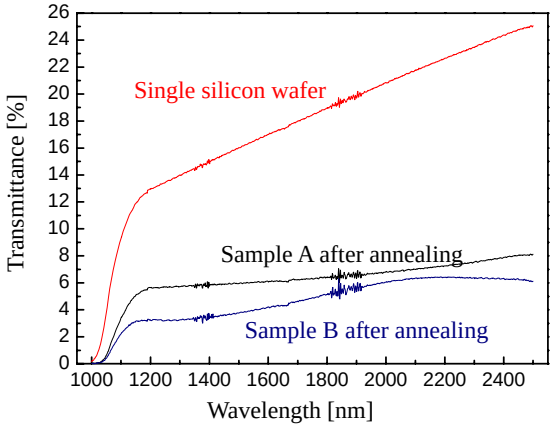
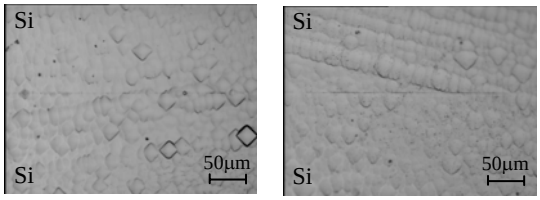


Fig. 4 Transmittance of the bonded wafer samples after annealing at 800ºC and single silicon wafer as a reference

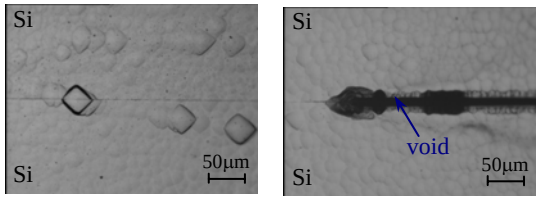
Figure 4 shows the transmittance of the samples A and B after 800ºC annealing. Voids at the interfaces lead to some gaps between the bonded wafers. Therefore, comparing to the sample A, the transmittance of the sample B behaves a wave-like shape as a function of wavelength.

10×10 mm^2 chip size samples, diced from the sample A and B, were stored in air at RT for 100 days, labeled as samples D and E respectively. The samples D and E were subsequent annealed at 700ºC for 2 h to investigate the void formation after this long time storage at RT. The voids are too small on chip-scale to be observed by IR camera. Thus, these samples were etched by 30% KOH solution at 90ºC for 3 min. For the sample D (pretreated by O_2 RIE 10s + N_2 radicals 60 s), no small voids are generated before and after 700ºC annealing as shown in Fig.5. For the sample E (pretreated by O_2 RIE 60s + N_2 radicals 60 s), voids appear clearly at the interface after 700ºC annealing [Fig.6(b)]. Therefore, the short O_2 RIE plasma pretreatment (~10 s) and followed by N_2 radicals for 60s is effective to mitigate/avoid annealing voids.



(a) (b)

Fig. 5 Bonded interfaces of the sample D after KOH etching (a) before (b) after annealing at 700 ºC for 2 h



(a) (b)

Fig. 6 Bonded interfaces of the sample E after KOH etching (a) before (b) after annealing at 700 ºC for 2 h

4. Conclusions

Si/Si direct bonding are performed by a shorter O_2 RIE pretreatment for 10 s and followed by N_2 radicals for 60 s. Strong bonding strength of Si/Si is achieved at RT as well as no voids generated in subsequent annealing process. We assume this sequential plasma activated process would be suitable for a void-free, room temperature bonding.

References

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