Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 426-427

P-3-11

Effect of STI Stress Enhanced Boron Diffusion on Leakage and Vcc_min of Sub-65nm node Low-Power SRAM

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ABSTRACT

A new finding and explanation of STI stress enhanced sidewall boron dopant diffusion effect on BTBT and Vcc_min of 65nm node low-power SRAM is presented. A significant increase of BTBT on STI edge sidewall was observed with non-optimized STI process, which suffers more seriously LOD effect. The defect enhanced boron diffusion model integrated the STI stress effect on defect generation is used to explain this observation. The BTBT degradation is attributed to the STI sidewall boron dopant enhanced diffusion and increased junction electric field of STI sidewall. This boron diffusion is random and more seriously in SRAM cell, thus results in worse pass-gate device mismatch and Vcc_min of 65nm node SRAM.

Keywords: STI stress, BTBT, defect enhanced boron diffusion model, Vcc_min, LOD effect.

I. INTRODUCTION

Leakage becomes serious issue as technology aggressively scales down, especially for low-power SRAM. Due to gate oxide scale down and increasing channel doping, both GIDL and BTBT (band-to-band leakage) become worse in sub-65nm node SRAM [1].

STI stress enhanced boron diffusion effect has been widely studied [2-3], most of them were focused on the effect to length on diffusion (LOD).The effect should be more significantly for small LOD and small width device such as SRAM device. However, so far, no further elaboration discussing on smaller area devices has been reported. In this work, we observed the STI stress generates defects along STI sidewall to enhance boron diffusion upstream to N+ junction, thus results in a higher electric field to cause high leakage. Besides, such boron diffusion leads the dopant fluctuation more seriously in SRAM device for its aggressed effective area.

II. EXPERIMENTAL

The SRAM and logic devices used in this work were fabricated with a 65nm leading-edge foundry low-power process. Two different STI processes A, and B were split to study STI stress effect. Both processes have almost same, except the process B has a lower thermal temperature to reduce the STI stress. **Fig. 1** shows TEM of these two different STI processes. Process A results in sharper STI corner and more STI oxide divot compared to process B as shown in Fig. 1. After STI process, 19A EOT GOX with 55nm gate length poly patterning process was used. Optimized source/drain extension and pocket implant was carefully designed to reduce GIDL and BTBT leakage in logic device and SRAM cell. STI sidewall's defects generated by STI stress were proposed with defect enhanced boron diffusion model to verify serious BTBT leakage of N+ junction to STI sidewall.

III. RESULTS AND DISCUSSION

Read current (I_{read}) vs. standby leakage current (I_{sb}) was also used to describe SRAM performance especially for low-power SRAM cell. Process B results in lower leakage with the same read current was observed as shown in **Fig. 2**. To investigate root cause of this improvement, LOD effect was studied. Process A shows more NFET's Ion degradation through LOD as shown in **Fig. 3**. Based on LOD effect, we could assume process A results in higher STI stress than process B. Scott et al.[5] indicates drive current and threshold voltage shifts result from stress induced dopant diffusion. We observed the same phenomenon in **Fig. 4**, STI stress does not impact on mobility through different LOD for both process A and process B for <100> channel direction wafer.

We also found larger STI stress increases STI sidewall junction capacitance as shown in **Fig. 5**(a). We proposed STI stress results in more defects along STI sidewall, and those defects enhanced boron diffusion upstream into N+ junction as shown in **Fig. 5**(b). This defect enhanced boron diffusion phenomenon results in higher N+ junction electric field along STI sidewall. **Fig. 6** shows device bulk leakage of different device width, process A that has larger STI stress results in higher junction bulk leakage in small width device. Larger STI stress results in large junction leakage of smaller width junction phenomenon shown in **Fig. 7** was also observed by Steegen et al.[4]. Because we used the same salicide process, this junction bulk leakage increase phenomenon correlates well with defect enhanced boron diffusion model because STI sidewall composes more area in small width device compared to large width device.

According to the above result, a defect enhanced boron diffusion model incorporating STI stress was proposed to explain the phenomenon. First, defects, which are generated from the STI mechanical stress in the STI sidewall regime, results in interstitials at the Si/SiO2 interface. Secondly, the generated defects enhanced boron diffusion. Stress enhanced dopant diffusion phenomenon had been pointed out by S. Chaudhry et. al[5]. In this study, we believed STI stress plays major role of enhanced boron dopant diffusion.

Process B had improved SRAM pass-gate device mismatch(defined as Vts difference of PG1/PG2) as shown in **Fig. 8**. There are two possible mechanisms could explain this phenomenon. The first mechanism is smaller STI divot difference by process B. since small width device is very sensitive to STI divot and smaller STI divot results in smaller device variation. The second mechanism is less boron channel dopant random distribution resulting from smaller STI stress by process B. Both mechanisms could explain why pull-down and pull-up device is not sensitive as pass-gate, since pull-down has larger active device area, so pull-down device should have the smallest mismatch among SRAM device. Regarding to pull-up device, channel dopant is As which is not easy to diffuse even under STI stress. The better random doping variation results in better SRAM device mismatch, and better device mismatch leads to better SNM(static noise margin) of SRAM[6-7]. For sub-65nm node, Vcc_min of SRAM had been widely discussed and SNM is strongly correlated to Vcc_min[8]. **Fig. 9** shows process B improve Vcc_min 50mV compared to process A, this phenomenon is well explained by better pass-gate device mismatch resulting from more healthy STI process B.

IV. CONCLUSIONS

A significant improvement of 65nm low power SRAM's Vcc_min and leakage current by properly manipulating STI process has been studied in detail in this work. We suspect the STI stress enhances the boron diffuses along STI sidewall to reach N+ source/drain junction, thus leads the increase of BTBT junction leakage. This phenomenon becomes worse as device width becomes smaller. With lower thermal temperature, the process B has less STI stress, smaller STI divot and more round STI corner, thus results in smaller SRAM leakage and junction bulk leakage. Furthermore, these factors also lead to insignificant boron dopant diffusion thus improving SRAM's device mis-match and Vcc_min with less pass-

gate device mismatch. Therefore, carefully optimizing STI process should become more important, and necessary for sub-65nm node.

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FIGURES

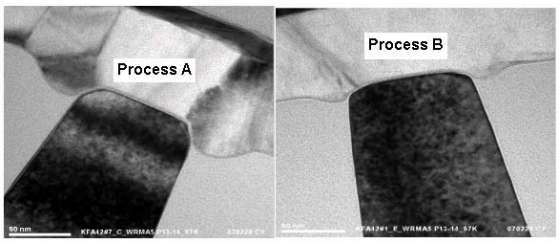
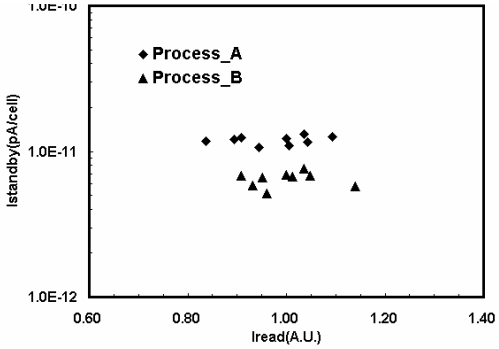


Fig. 1 Cross-section TEM pictures of process A and process B, process A shows more serious STI divot and sharper STI corner .

Fig. 2 I_{read} and $I_{standby}$ of 65nm low power SRAM cell(cell size=0.525um^2).



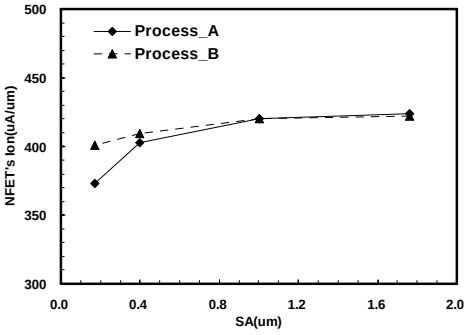
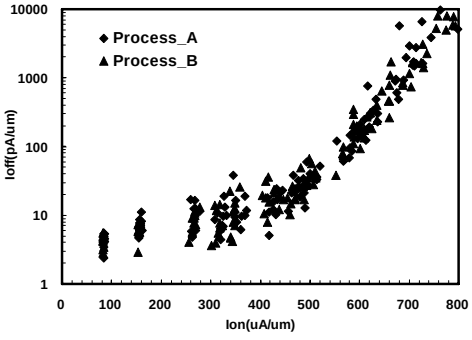


Fig. 3 NFET's LOD effect of STI process A and process B.



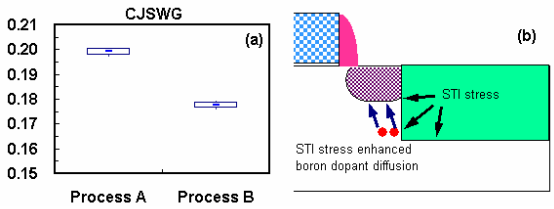


Fig. 5 (a)Poly gate sidewall junction capacitance of splits(b)STI stress enhances channel boron dopant diffuse along STI sidewall to N+ source/drain junction.

Fig. 4 NFET's Ion/Ioff of STI process A and process B.

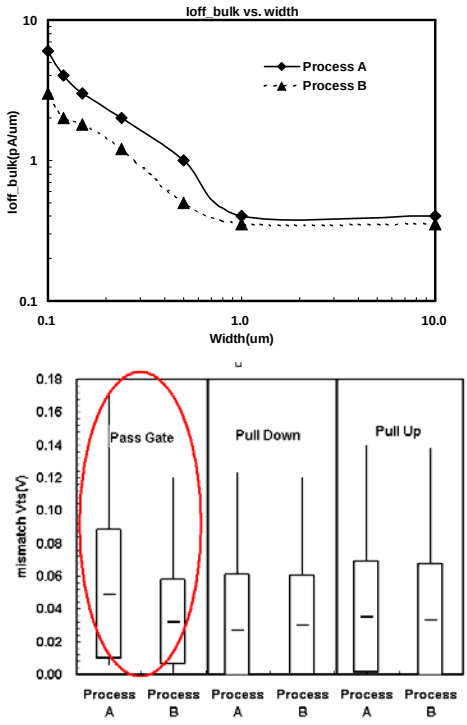


Fig. 6 Bulk leakage through width with STI process splits.

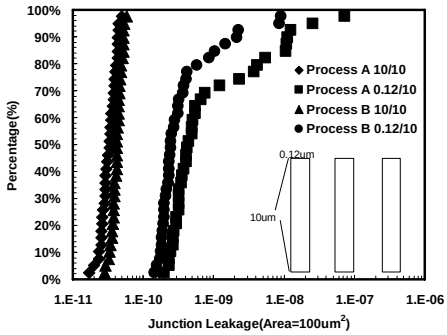


Fig. 7 Junction leakage of diode with different STI process.

Fig. 8 SRAM device mismatch of process A and process B.