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The Effect of Etch Stop Layer Stress on Negative Bias Temperature Instability of Deep Submicron p-MOSFETs

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Abstract

NBTI (Negative Bias Temperature Instability) in dual gate oxide CMOS process causes Vt shift and has become a crucial challenge in the design of the advanced analog or mixed signal circuit. In this letter, the impact of the stresses from contact etch stop layer (CESL) on the NBTI of p-MOSEFET's I/O (input-output) was investigated in detail. Experimental results show that the tensile stress has about 5 times ability to suppress Vt shift caused by NBTI in comparison to that of compressive stress, thus becomes a simple and effective method to relieve NBTI.

I. Introduction

In the advanced analog and mixed signal circuit CMOS, dual gate oxide layer composed of two different thickness may be formed within a single chip in order to maintain each of the characteristics of the merged devices. In such devices, NBTI (Negative Bias Temperature Instability) will cause various device parameters degradation such as threshold voltage shift, thus becoming a critical challenge in design of these circuit CMOS [1-3]. In the past, many approaches have been reported to relieve NBTI such as introduction of fluorine [4], performing the NO anneal process before oxidation [5], using O3 pre-treatment and pulse-time-modulated beam injection [6-7]. However, we have found even the stresses from contact etch stop layer (CESL) degrade PMOS drive current but the tensile stress can also effectively suppress NBTI. In this work, we systematically studied and compared the impact of compressive and tensile stresses of CESL on dual gate oxide I/O p-MOSFETs with various channel length and width. Additionally, the mechanism of NBTI caused frequency-dependent Vt shift was investigated and found the complex interplay of reaction-diffusion limit trap generation process [8] dominates the NBTI caused Vt shift degradation.

II. Device Preparation and Measurements

The samples for this study were prepared with conventional 0.13 CMOS dual gate oxide process including 1.2V (thin gate oxide) and 3.3V (thick gate oxide). Firstly, the thick gate oxide (6.5nm) was thermally grown under 1050 degree C. Next open 1.2V (thin gate oxide) area by Lithography and removed the gate oxide on 1.2V area by Etch. Then, removing Photo-resistor and re-grown the real thin gate oxide (in both 1.2V/3.3V areas.) After gate deposition, optimum device implantations for 1.2V & 3.3V MOSFET were executed sequentially and followed by PECVD deposition of various SiN films for ILD contact etch stop layers on different samples. By manipulating the UV curing and SiH4/NH3 flux, the SiN CESL films can be formed with compressive, tensile, and high tensile stresses, respectively. Finally, completed the samples through backend processes shown in Table 1. During the processing, the steps including coating photo resister, defining thick gate oxide and open thin gate oxide, and removing thick gate oxide are harmful to the interface between gate oxide and channel thus enhancing the generation of NBTI. The measurement of NBSI is executed through the evaluation of the stability of transistor's threshold voltage as subjected to accelerated stress condition of 1.4 times Vg @ 125 0 C, 3 dies for each stress voltage, 10000 seconds per die. On the other hand, Vt is measured by constant current method with Agilent 4073 semiconductor parameter test system.

III. Results and Discussions

Figure.1 compares the Vt shift of 3.3V p-MOSFET with different CESL films. The data were measured by DC NBTI stress (constant voltage and temperature). Figure.2 shows the log-log plot of Vt shift vs stress time. As seen, Vt shift of 3.3V p-MOSFETs is worse with compressive stress SiN film but less with tensile stress SiN film. For example, about 44% and 60% reduction in Vt shift are found for the tensile stress (0.3Gpa) and high tensile (0.5Gpa) SiN film compared to that of compressive stress (-0.5Gpa) respectively. Table.2 Next, Figs.3 ,4 ,5, and 6 show the threshold voltage (Vt) and saturation current (Idst) characteristics of 3.3V n-MOSFETs and p-MOSFETs with different channel width and CESL films, respectively. Based on the device characteristics, the tensile stress film enhances the electron mobility and thus the saturation current of nominal 3.3V n-MOSFETs (W=10um/L=0.34um) about 7% and not obvious degradation (about 3%) for p-MOSFETs current. The most important is the tensile stress film does not worse Vt roll-off for both short channel n-/p-MOSFETs. Therefore, to simplify manufacture process the CESL film with tensile stress should be used for both 3.3V p-MOSFETs and n-MOSFETs.

Additionally, to realize the origins of different impact of CESL film stresses, the dynamic (AC) NBTI stress was implemented. In which, the measurement of Vt shift is separated into stress and relax periods. In the past, it has been reported [10-11], when a pMOSFET is biased in inversion mode, the holes in the inversion layer will interact with the Si-H bonds at the channel-oxide interface and weaken the Si-H bonds under stress period (voltage, temperature) to lead dissociation of H atoms and thus generating interface traps (Nit). Subsequently, the period of relax coming in and all the stresses are released. Meanwhile, the dissociated H atoms near the interface now rapidly recover the broken Si-H bonds to anneal the Nit and lower the Vt shift again. Fig.7 shows the Vt shift versus stress time under the dynamic NBTI for dual gate oxide p-MOSFET with split the CESL stresses. As seen, under tensile stress, more slowly rising in Vt shift in stress period and quickly lowering down in the relax period in comparison to that of compressive stress are found. This means the Si-H bonds are harder to dissociate and easier to bond for tensile stress film than that for compressive stress film as Figure 8. Moreover, the stress effect on the dissociation or bonding of Si-H bonds is more significantly for high tensile stress. In other words, tensile stress especially for high tensile stress is better benefit to NBTI for its higher ability to suppress Si-H bonds dissociation.

VI. Conclusion

The stress effect of cont etch stop layer deposited by PECVD on DC/AC NBTI, saturation current of dual gate oxide I/O p/n-MOSFET's

with different channel length have been studied in detail. The NBSI was measured through the evaluation of the stability of transistor's threshold voltage as subjected to accelerated stress condition. The DC NBTI test find that the tensile stress film enhances the Idsat of I/O n-MOSFETs about 8% and does not worsen the short channel Vt roll-off. Meanwhile, even tensile stress film leads to the 3% decrease in Idsat of I/O p-MOSFETs, but it improves the Vt shift caused by NBTI around 60%. Besides, the AC NBTI test find the Si-H bonds dissociation dominates the effect of stress condition on NBTI.

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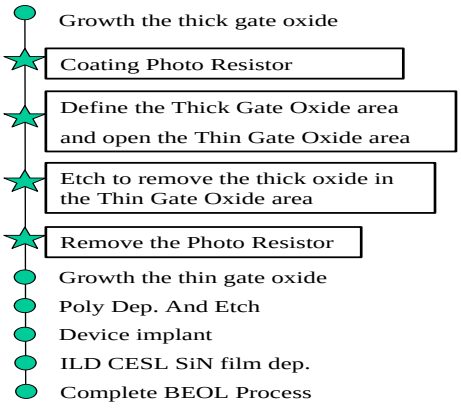

Table. 1 The brief process for Dual gate oxide. Four steps (star mark) are harmful for Gox interface.

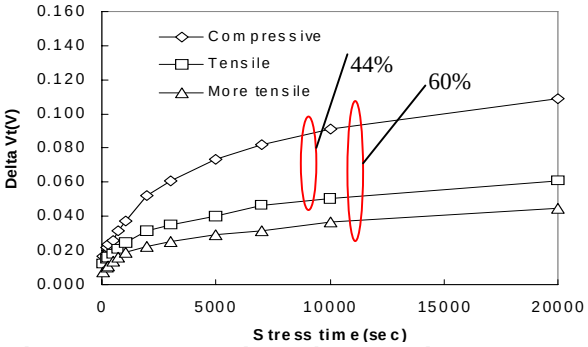

Fig.1 Delta Vt vs stress time under 125degree C and various SiN CESL stress.

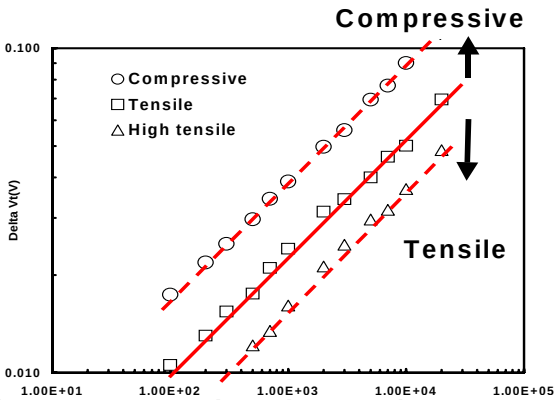

Fig.2 Delta Vt vs stress time under 125degree C and various SiN CESL stress (log-log plat).

	Compressive	Tensile	High tensile	Unit
Stress	-0.50	0.30	0.50	GPa
Delta Vt	0.109	0.061	0.045	Volt

Table. 2 The Vt shift is disproportional to stress.

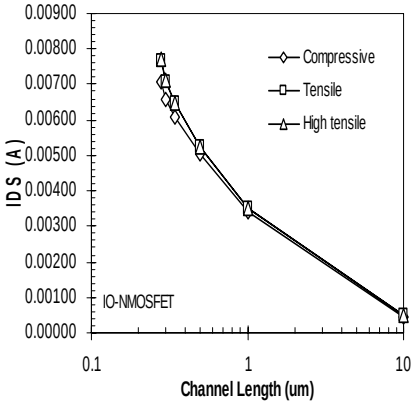

Fig. 3 IO-NMOSFET IDS vs channel length in Dual gate Oxide process.

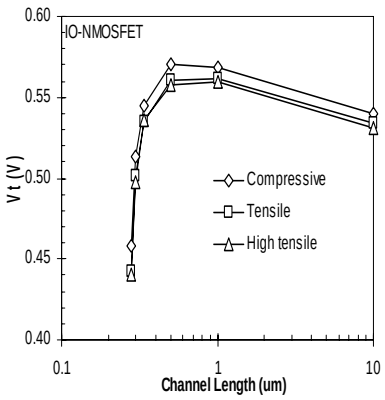

Fig. 4 IO-NMOSFET Vt vs channel length in Dual gate Oxide process.

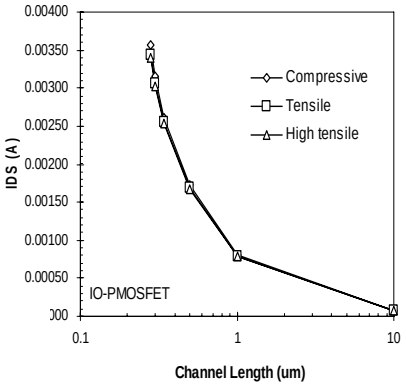

Fig. 5 IO-PMOSFET IDS vs channel length in Dual gate Oxide process.

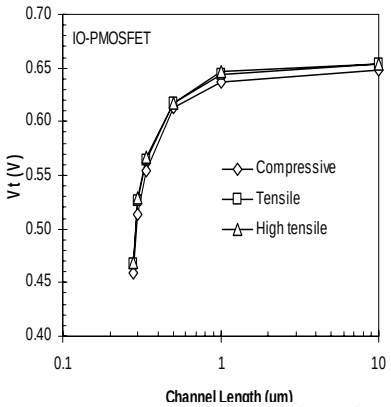

Fig. 6 IO-PMOSFET Vt vs channel length in Dual gate Oxide process.

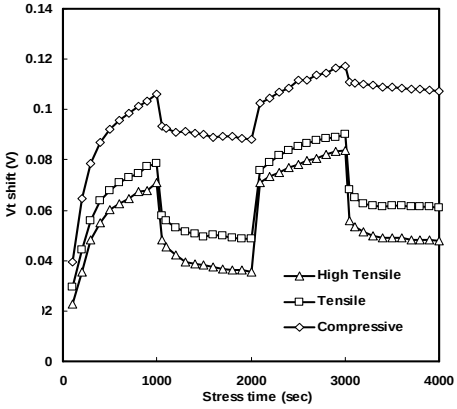

Fig. 7 Delta Vt vs stress time under the dynamic NBTI test with various stress for dual gate oxide I/O pMOSFET.

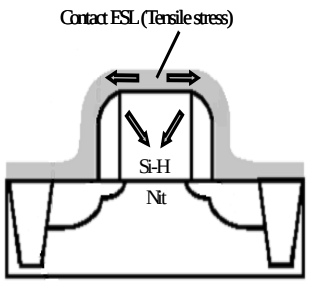

Fig. 8 The Si-H bonds are harder to dissociate and easier to bond for tensile stress film