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Enhanced NBTI Degradation by SMT in Short-Channel pMOSFET

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Introduction

Mobility enhancement from the introduction of stressor has received a lot of attention. Stressors can be introduced in two main forms: substrate-strain based or process-induced strain based. The substrate-strain based makes use of material with different lattice spacing, such as SiGe/Si epitaxial stack to generate biaxial strain in the channel. This method introduces a global strain to the substrate. It boosts mobility effectively but at a higher cost [1]. On the other hand, process-induced strain based method provides a lower cost solution. They could appear in the forms of shallow trench isolation (STI), contact etching stop layer (CESL) and stress memorization technique (SMT), which introduce uniaxial strain to boost mobility [2-5]. Both nMOSFET and pMOSFET have different requirements in strain. nMOSFET performed better under the presence of tensile strain, while pMOSFET performs better under the compressive strain. This article reveals that SMT enhances nMOSFET's performance. Nevertheless, the gain will be achieved at the expense of poorer pMOSFET's performance and reliability, particularly when the device dimension is continued being scaled.

Experiment

The MOSFETs used in this work were fabricated using conventional CMOS processes. SMT stack layer was introduced after source/drain implantation and followed by high temperature activation. Process details can be found elsewhere [6]. The impact of SMT process to device performance was examined from device's transfer characteristics. Since NBTI is of growing importance for modern ICs [7-8], the impact of SMT on NBTI will be the key focus in this paper. Charge pumping measurement will also be performed to substantiate the NBTI results.

Results and Discussion

Figure 1(a) shows the linear mode Id-Vg for nMOSFET with and without SMT, at a drain voltage of 0.05V. Figure 1(b) compares the corresponding mobility, as inferred from $Gm_{max} \times T_{ox}$ parameters. It is evident that the incorporation of SMT boosts the device performance for nMOSFET. The SMT layer introduces an uniaxial tensile strain along the channel direction and enhances electron mobility. Figure 2(a) shows the linear mode Id-Vg for a pMOFET with and without SMT, measured at Vd = -0.05V. Similarly, fig. 2(b) compares the holes mobility from $Gm_{max} \times T_{ox}$ parameters for pMOSFET. Result shows the introduction of SMT degrades pMOSFET performance by lowering holes mobility. In summary, the introduction of SMT produces tensile strain in the direction of channel. This tensile strain boosts electrons mobility but "retards" holes mobility. Figures 3 and 4 show the Id-Vd plots for both nMOSFET and pMOSFET, respectively. Both were plotted to compare the effect of SMT. Device with SMT was found to enhanced Id-Vd performance, valid for both nMOSFET and pMOSFET. This is consistent with the observations in Figs.1 and Figs.2. Again, the different observation could be attributed to the presence of tensile strain, introduced by SMT.

In addition to device performance, the impact of SMT to NBTI was also assessed. The NBTI stressing was performed under a constant negative gate biasing with the source, drain and substrate terminals grounded. Stressing was carried out at elevated temperature of 125^{O}C. Device is considered failed when its Idsat drifts by 10% from its initial value. Figure 5 shows the NBTI lifetime for various channel lengths. In general, NBTI improves as the channel length shrinks progressively. This trend is valid, independent to whether SMT has been added onto the device. On the other hand, it is observed that for long channel device, SMT has negligible effect onto NBTI lifetime. However, as the channel length shrinks progressively, the impact of SMT onto NBTI lifetime becomes more evident. Device with SMT incorporated exhibits a much worsens NBTI lifetime. NBTI degradation has been correlated to the generation defects at the Si/SiO2 interface during electrical stress. Interface traps could exist in the form of silicon trivalent dangling bonds [6-7]. The presence of tensile strain, introduced by SMT, could enhance the interfacial hydrogen release to form more interface traps than that without SMT. For long channel device, the difference in strain could be relatively smaller. As the channel length is being scaled down progressively, the difference in strain will be magnified and reflected as worsens NBTI. To substantiate this model, charge-pumping measurement was performed on these devices.

Figure 6 shows the charge-pumping current density as a function of base voltage. Initial interface traps density (Dit_0) could be inferred from the maximum Icp, measured on fresh device. Figure 7 compares the initial interface traps density for pMOSFETs, with and without SMT. Results are plotted for various channel lengths. Dit_0 level decreases with channel length, independent to whether SMT has been incorporated. This is consistent with Fig. 5 data, showing better NBTI performance at shorter channel length. On the other hand, comparing samples with and without SMT, the difference in Dit_0 is found to become larger as channel length shrinks. This verifies our model that the difference in tensile strain will be "felt more strongly" as the channel length shrinks. The key implication of this finding is that SMT incorporation boost nMOSFET's performance but it degrades pMOSFET's performance and NBTI at the sametime. Degradation will be further enhanced as the device dimension continues to be down-scaled. So, removing the SMT over pMOSFET could be an option to bypass these issues.

Figure 8 shows the lifetime of NBTI as a function of gate biasing for pMOSFET with short channel length of 0.06 μm. Devices with SMT device, has their NBTI lifetime deteriorates by 2-3 times. This result shows that if we pay much attention to nMOSFET performance improvement and ignore the tensile stress impact in pMOSFET, it will not only degrade CMOS performance but also bring on reliability issues.

Conclusion

This article reveals that the SMT process increases the nMOSFET electrical performance (Id-Vg and Id-Vg) but at the expense of device performance and NBTI reliability for pMOSFET. In this study, we also clarified the dependence of NBTI on channel length. The incorporation of SMT causes more severe impact on pMOSFET, particularly when the device is continued becomes smaller.

Reference

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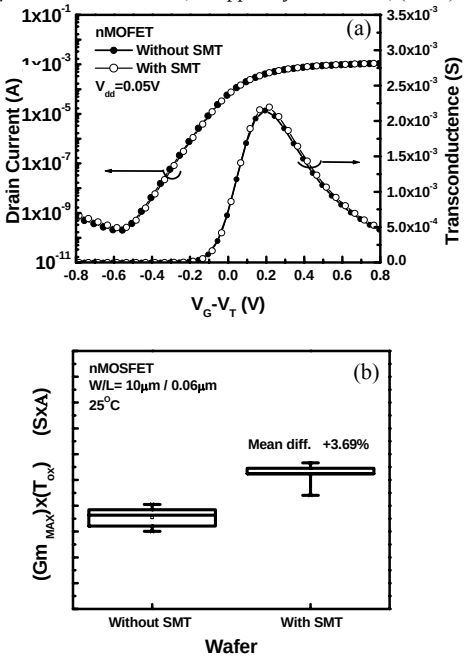

Figure 1: Comparison of (a) linear mode transfer characteristic (Id-Vg) and (b) mobility for nMOSFET with and without SMT

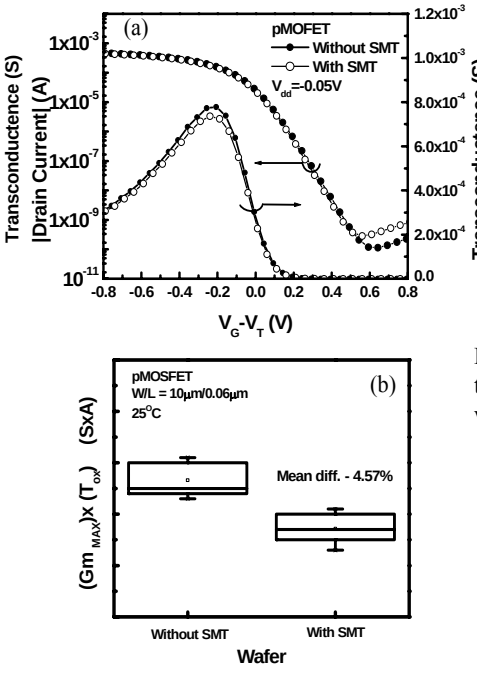

Figure 2: Comparison of (a) linear mode transfer characteristic (Id-Vg) and (b) mobility for nMOSFET with and without SMT

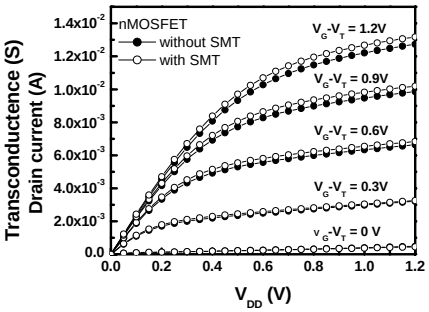

Figure 3: Comparison of Id-Vd to show the difference for nMOSFET with and without SMT.

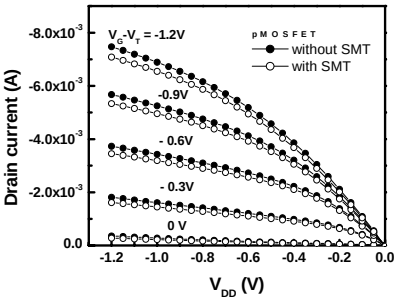

Figure 4: Comparison of Id-Vd to show the difference for nMOSFET with and without SMT.

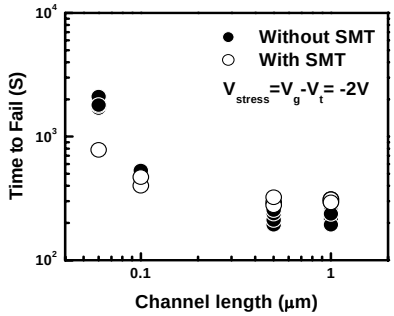

Figure 5: NBTI lifetime comparison for samples with and without SMT. Comparison was made for different channel lengths. Measurement was performed at 125°C.

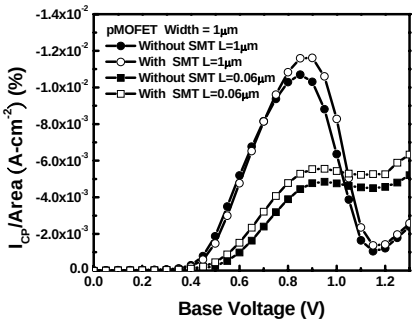

Figure 6: Charge-pumping current versus base voltage for pMOSFET with and without SMT. Comparison was made for long channel and short channel devices.

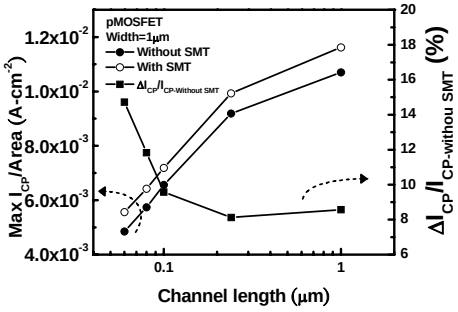

Figure 7: Maximum charge pumping current as function of channel length. The difference (comparing with SMT to without MST) in charge-pumping current becomes more evident for shorter channel length.

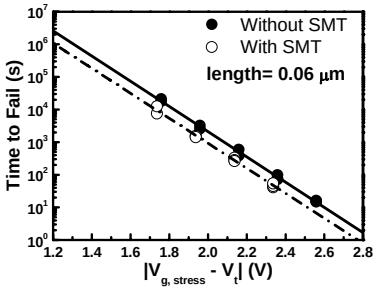

Figure 8: Comparison of NBTI lifetime for short channel devices with and without SMT. Introduction of SMT degrades NBTI by 2-3 times (Temperature=125°C, channel length=0.06um)