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Effects of hot carriers on DC and RF performances of deep submicron PMOSFET for low-power and high frequency applications

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1. Introductions

Generally, the cutoff frequency Ft and maximum oscillation frequency Fmax are the figure of merit (FOM) for RF performances of CMOS devices. They reach the range of hundred GHz as the gate lengths of CMOS devices scale down to the deep submicron region, and make them to be attractive and as the best choice for low-power and high-frequency applications. However, as the gate length keeps scaling, the unchanged power supply will cause high lateral field and thus the creations of hot carriers. These hot carriers will result in the damages, comprising of interfaces and oxide traps, near the drain side and thus degrading both the DC and RF performances [1][2]. In the past, many researches paid more attentions on NMOS since it has more serious hot carriers effects than PMOS. However, the influences of hot holes arise fast as the gate length of PMOS reach deep submicron region. Hence, in this work, we investigate the effects of hot holes in detail on deep submicron PMOS.

Three bias stresses were used to investigate the hot carriers effects, i.e., stress Vg equaling to stress Vd, peak substrate current Ib, and stress Vg around threshold voltage Vt [3]. After constant voltage stressing, not only DC but also RF parameters will be degraded due to the induced damages near the drain side. The worst case among these three mechanisms will be discussed in this paper.

2. Experiments

65 nm PMOS devices with gate length of 0.06 um were picked up to investigate the hot carriers effects. To save the area of test-keys, the DUTs (devices-under-test) were laid with the pad structures of in-line GSSG (Grounding-Signal-Signal-Grounding), which is suitable especially for RF automatic measurement, RF automatic measurements by semi-auto RF testing system (Cascade S-300 with Agilent PNA and 4156C) with the proprietary ICCAP control program were used to save human load and measurement time [4]. Three dies were measured and averaged to get the accurate results. Gate and drain were connected to top and bottom signal pad, respectively; whereas source and substrate together to ground pad. For peak Ib mechanism, since Ib could not be measured for the GSSG pad structure, stress Vg equaling to half of stress Vd was selected and it was believed to have the similar results as that of peak Ib. Various stress time, 40 min, 80 min and 120 min were used. After stressing, DC and RF measurements were implemented immediately without probes lifts to keep the same contact resistances and from recovery effect.

Scattering parameters (S- parameters) were measured under 2.5 GHz and converted to common RF parameters by Kwon's model [5]. Two dummy patterns, OPEN and SHORT, were used for accurate de-embedding. Methods of LRRM (Line-Reflect-Reflect-Match) were used for accurate calibrations.

3. Results and Discussions

Figure 1 shows the drain current Id versus gate voltage Vg before and after various stress time for the case of stress Vg = stress Vd = 1.8 V. It can be seen that the degradation caused from the hot carriers increases as stress time increases. The threshold voltage Vt is enhanced after stressing and thus resulting in the degradation of transconductance Gm as shown in Fig. 2. It should be noted that the maximum degradation of Gm occurs near half of Vcc and this region is the usual operation region for analog circuits. Since the cutoff frequency Ft and maximum oscillation frequency Fmax are both dependent on Gm, Figs. 3 and 4 show the degradations of Ft and Fmax with the same trend. These relations of Ft and Fmax to Gm can be seen in Figs. 5 to 6. As stress time increases, the slopes of Ft to Fmax to Gm show very little decrease, and it means the denominators of equations (1) and (2) keep little increase or unchanged after stressing.

$$f_T = \frac{g_m}{2\pi\left(C_{gd} + C_{gs}\right)} \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

$$f_{\max} = \frac{f_T}{2\sqrt{g_{ds}R_{in} + 2\pi f_T R_G C_{gd}}} \quad (2)$$

To investigate the worst case among the three common stress mechanisms, Fig. 7 shows the Id degradation versus stress time as the function of mechanism. It is obvious that the mechanism of stress Vg equaling to stress Vd is the worst case. In previous CMOS technology, the worst case is usually the peak Ib; however, it has been changed to that of stress Vg = stress Vd as the process technology advance to sub-micron region. Figs. 8 to 10 show the similar results for Gm, Ft and Fmax. In addition, the degradation decreases as the stress time increases. This means the most damages were caused in early stress and would reach the saturations after many stresses.

The stress voltage effect on the Id, Gm and Ft degradation are shown in Figs. 11 to 13, respectively. As stress voltage increases, there is little increase for the degradation slope. It may cause from not only hot carriers effects but also oxide soft breakdown. Since Ft is the FOM of RF devices, not only the degradation limit of Id but also that of Ft can be extrapolated to decide the lifetime.

4. Conclusions

Hot carriers effects in deep submicron PMOS with in-line GSSG pad structure for saving test-key area and measurement time have been studied in detail, and found not only DC but also RF parameters are degraded seriously. Besides, we observed the stress condition for the worst degradation is changed to Vg = Vd, which is different to the conventional Vg=1/2 Vd.

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References

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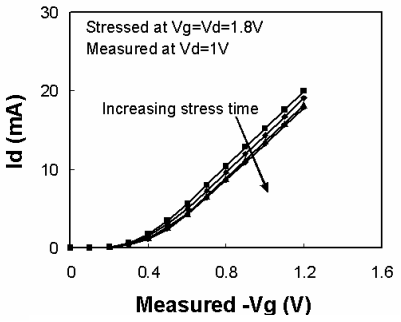

Fig.1 Id-Vg curve before and after various DC stress duration.

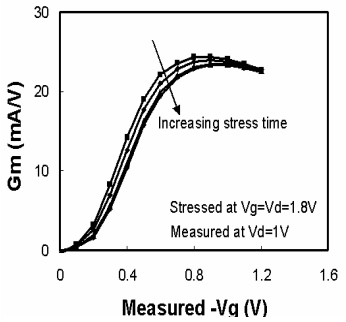

Fig.2 Gm-Vg curve before and after various DC stress duration. Gm degradations occur around Vg = 0.5Vcc.

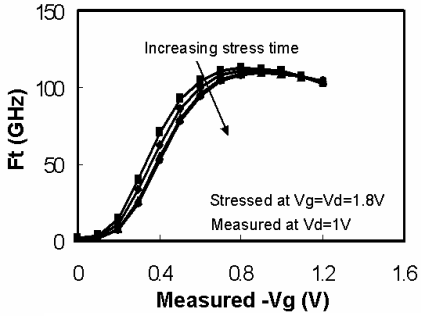

Fig.3 Ft-Vg curve before and after various DC stress duration. Ft degradation is dependent strongly on that of Gm.

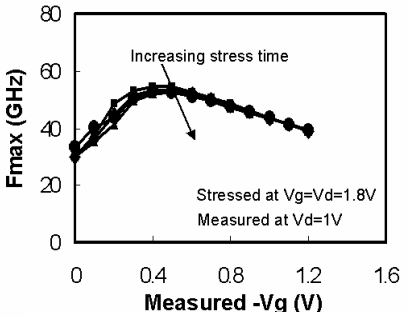

Fig.4 Fmax-Vg curve before and after various DC stress duration.

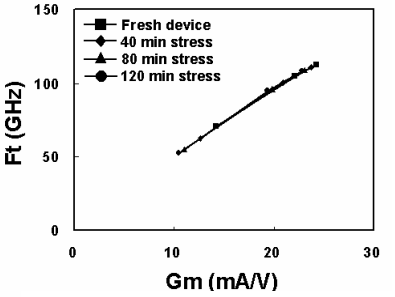

Fig.5 Ft-Gm curve before and after various DC stress duration. The very little slope decrease means that the gate capacitance keeps unchanged after stress.

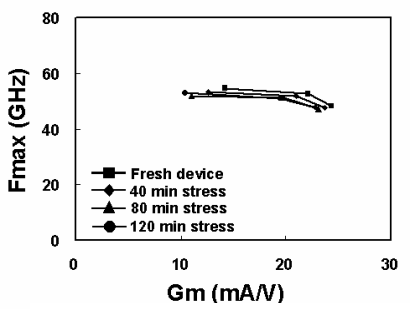

Fig.6 Fmax-Gm curve before and after various DC stress duration.

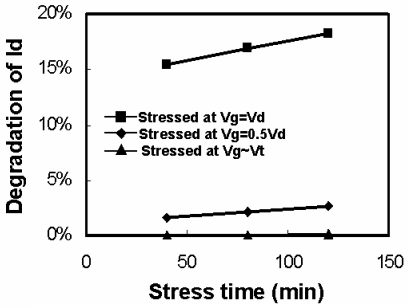

Fig.7 Id degradation after various DC stress duration. Stressed Vd=1.8 V

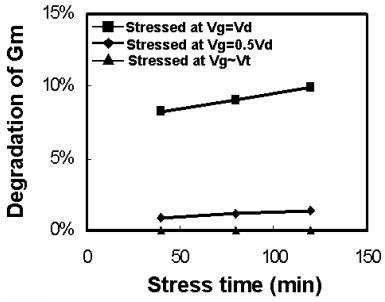

Fig.8 Gm degradation after various DC stress duration. Stressed Vd=1.8 V

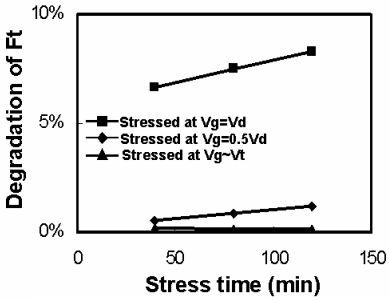

Fig.9 Ft degradation after various DC stress duration. Stressed Vd=1.8 V

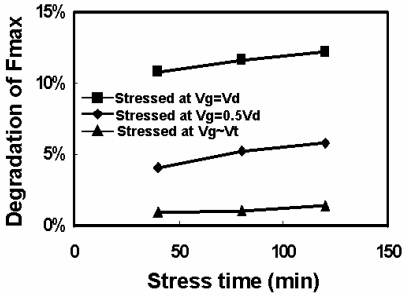

Fig.10 Fmax degradation after various DC stress duration. Stressed Vd=1.8 V

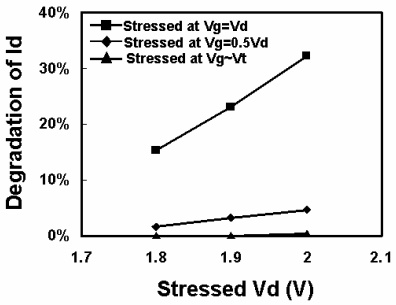

Fig.11 Id degradation for various DC stressed Vd. Stressed duration is 40 min.

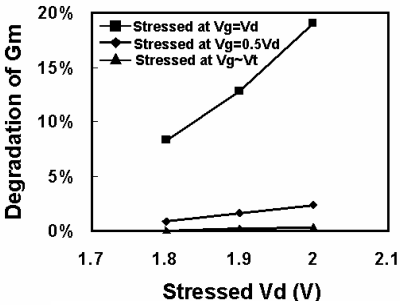

Fig.12 Gm degradation for various DC stressed Vd. Stressed duration is 40 min.

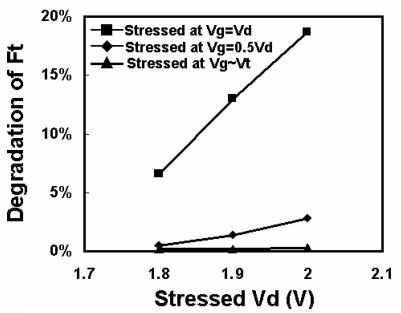

Fig.13 Ft degradation for various DC stressed Vd. Stressed duration is 40 min.