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NBTI-Stress Induced Grain-Boundary Degradation in Low-Temperature Poly-Si Thin-Film Transistors

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1. Introduction

Low-temperature poly-Si TFTs (LTPS TFTs) have been widely studied for their possible realization of system on panel (SOP). To be used in the driving circuit, high reliable LTPS TFTs are required. Okuyama *et al.* have pointed out that NBTI stress causes performance degradation in TFTs [1]. However, the detail degradation of LTPS TFTs under NBTI stress, especially the role of grain boundary, is still not clearly studied. Therefore, we applied different methods to identify the grain-boundary degradation in LTPS TFTs under NBTI stress.

2. Experimental

P-channel LTPS TFTs were fabricated on glass substrates. First, a 40nm-thick amorphous-Si layer was deposited and crystallized into poly-Si film by excimer laser annealing. Then, gate dielectric was deposited with an equivalent 100nm-thick SiO_2 layer and followed by Mo deposition as gate electrode. After gate patterning, source and drain were doped by plasma doping. Hydrogenation was performed with NH_3 plasma treatment to passivate the dangling bonds. Inter-layer dielectric was deposited and densified. Finally, after contact hole opening, metal pad was deposited and patterned. The channel length (L) and width (W) of the device used in this study were 10 and 20 μm, respectively. Besides, some devices were fabricated with substrate contact for charge-pumping measurement.

The schematic cross-sectional view of the LTPS TFT and the stress setup is shown in Fig. 1. The NBTI stress was performed with a voltage of −15 to −30 V applied to the gate while the source and drain were grounded, and the glass substrate was heated to the stress temperature ranging from 25 to 150 °C.

3. Results and Discussion

Figs. 2 (a) and (b) show the transfer and output characteristics of the LTPS TFT, respectively. After the stress, the threshold voltage (V_{th}) shifts to be more negative, and the transconductance and subthreshold swing slightly degrade. Besides, the driving current decreases after the NBTI stress as shown in Fig. 2 (b). To characterize the degradation mechanism, the time dependence of the threshold-voltage shift (ΔV_{th}) is plotted as shown in Fig. 3. The ΔV_{th} follows a power law dependence on the stress time (t) with an exponent factor of 0.28 to 0.34, which is similar to the results previously reported in MOSFETs [2][3]. The exponent value of about 1/4 to 1/3 is generally explained as the diffusion-controlled electrochemical reactions, which originate from the depassivattion of hydrogen in the dielectric/channel interface.

In LTPS TFTs, there are many grain-boundary trap states in the channel film, which may be initially passivated during the hydrogenation process. However, we speculate that the depassivation of hydrogen atoms in the grain boundaries could happen during the NBTI stress. Therefore, we extracted the grain-boundary trap-state density (N_{trap}) by Levinson and Proano method [4][5]. Fig. 4 exhibits the plots of ln $[I_{DS} / (V_{GS} - V_{FB})]$ versus $1 / (V_{GS} - V_{FB})^2$ curves. It is apparent that the N_{trap} increases indeed after the NBTI stress, indicating grain-boundary trap-state generation must be considered in the NBTI-degradation for LTPS TFTs. Fig. 5 shows the time dependence of the ΔN_{trap} at 100 °C with various stress voltages. It is found that the ΔN_{trap}, like the ΔV_{th}, follows a power law dependence on the stress time with an exponent factor of 0.25 to 0.32.

To further confirm the role of the grain boundary in the NBTI degradation, the charge-pumping current (I_{CP}), which has been reported to derive the grain-boundary trap properties of poly-Si TFTs [6], was measured to identify the the grain-boundary degradation. Fig. 6 shows the I_{CP} of the device before and after 1000-s NBTI stress measured under the frequency of 1 MHz with fixed pulse amplitude of 1.5 V. The maximum I_{CP} increases after NBTI stress, indicating that the N_{trap} increases. Besides, the curve of the I_{CP} shifts to the negative direction, this implies that NBTI stress generates fixed-oxide charges in the device. Figs. 7 (a) and (b) show the time dependence of the ΔI_{CP} with various stress voltages and temperatures, respectively. The ΔI_{CP} also follows a power law dependence on the stress time. Besides, the ΔI_{CP} increases with the stress voltage and stress temperature, and this is because NBTI degradation can be electrically and thermally activated. Fig. 8 shows the correlation between the ΔI_{CP} and ΔV_{th}, Both the two physical quantities are closely related, therefore, we have demonstrated that the grain-boundary trap-state generation occurs in the NBTI degradation of LTPS TFTs.

Fig. 9 shows the schematic diagram illustrating the NBTI degradation in LTPS TFTs. During NBTI stress, the hydrogen atoms at the poly-Si/SiO_2 interface and in the grain boundaries dissociate from the Si atoms, resulting in the generation of interface trap states and grain-boundary trap states. The released hydrogen species diffuse or drift into the gate oxide and react with it, forming OH groups bounded to oxide Si atoms and leaving positive fixed-oxide charges. Finally, the hydrogen species diffuse in the gate oxide, becoming the reaction-limiting factor.

4. Conclusion

The role of grain-boundary trap-state generation during NBTI stress has been identified in this study. We conclude that the generation of interface trap states, grain-boundary trap states and fixed-oxide charges during the NBTI stress contributes to the threshold-voltage shift and degrades the reliability of LTPS TFTs.

Acknowledgements

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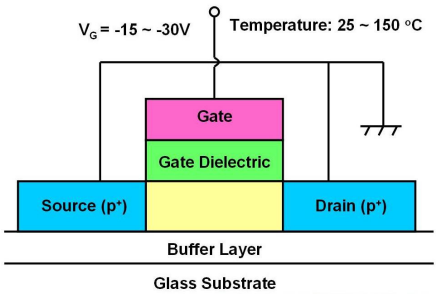

Fig. 1 Schematic cross-sectional view of the LTPS TFT and the stress setup.

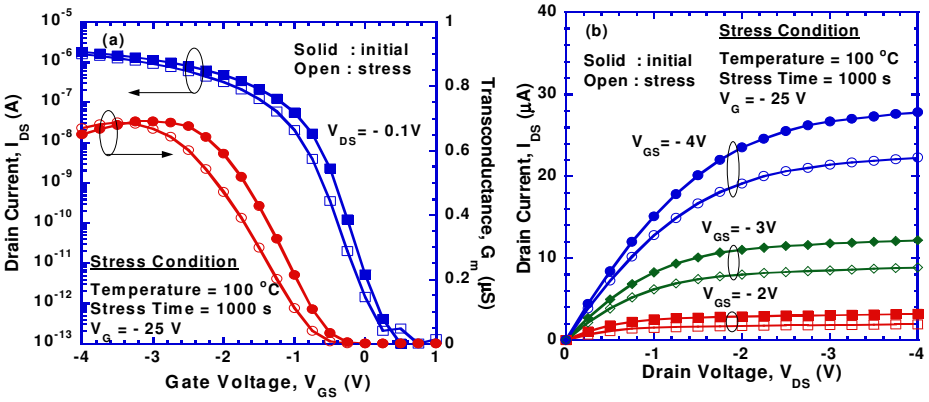

Fig. 2 (a) Transfer and (b) output characteristics of the LTPS TFT before and after 1000-s NBTI stress at 100 °C.

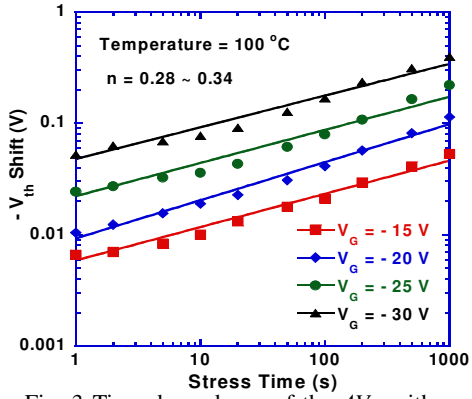

Fig. 3 Time dependence of the ΔV_{th} with various stress voltages at 100 °C.

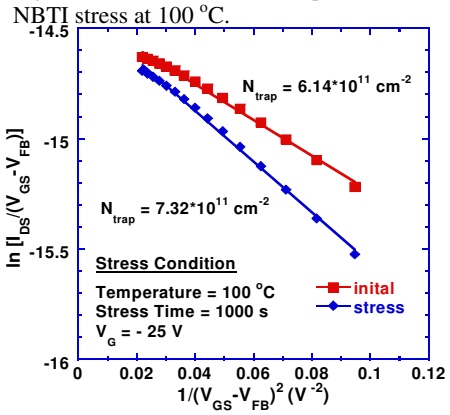

Fig. 4 Grain-boundary trap-state density extraction of the LTPS TFT.

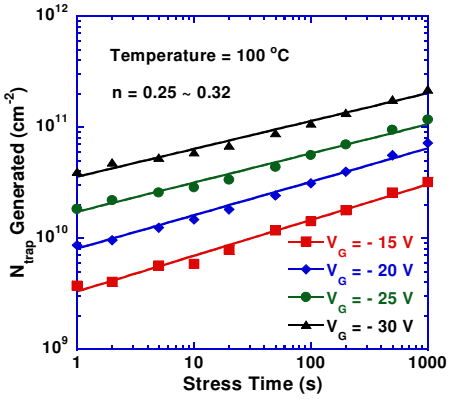

Fig. 5 Time dependence of the ΔN_{trap} with various stress voltages at 100 °C.

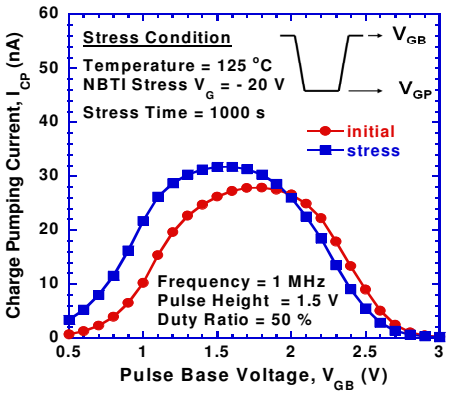

Fig. 6 Charge-pumping current before and after NBTI stress at 125°C.

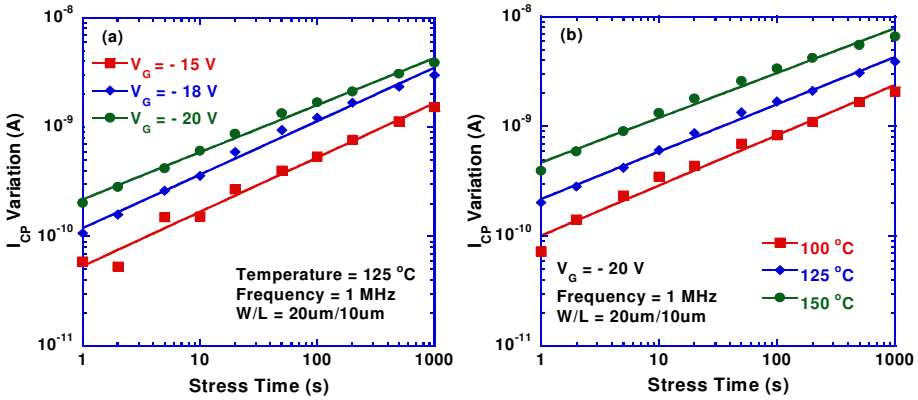

Fig. 7 Time dependence of ΔI_{CP} with various (a) stress voltages and (b) stress temperatures.

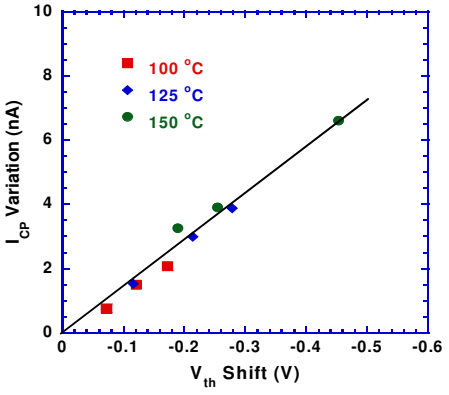

Fig. 8 Correlation between ΔI_{CP} and ΔV_{th}.

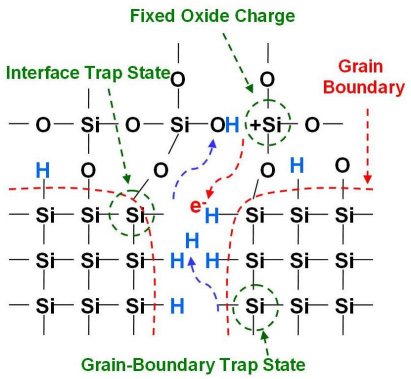

Fig. 9 Schematic diagram illustrating the NBTI degradation in LTPS TFTs.

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