P-3-20

# Determining the Gate-Finger Width for the Minimum Gate Resistance in RF MOSFETs

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## 1. Introduction

Owing to the importance of considering gate resistance ($R_g$) for radio-frequency (RF) and noise modeling, several studies have been reported to determine its value [1]-[9]. It has been known that the advanced $R_g$ model by considering the distributed effect of the gate electrode and non-quasi-static effect in the channel is necessary to describe accurately the RF behavior of MOSFETs [1]-[4] .

To understand and find the optimum gate-finger width ($W_f$) specially related to the distributed gate electrode resistance ($R_{ele}$) which includes both gate silicide resistance ($R_{sh}$) and silicide-to-polysilicon contact resistance ($\rho_{cnt}$) , the analysis with extra test structures or simulation has been performed in [3]-[6]. Because of some difficulty in distinguishing between $R_{sh}$ and $\rho_{cnt}$, it required special test vehicle and complicated structures [5], [6].

In this paper, we extracted both $R_{sh}$ and $\rho_{cnt}$ directly with 65-nm technology in RF MOSFETs and compared them with results of 130nm technology. The optimum finger width was obtained by analytical equation for NMOSFETs and PMOSFETs.

## 2. Experiments and model

The *S*-parameters of 65-nm dual gate RF MOSFETs with Ni-salicided polysilicon were measured at a frequency range from 100 MHz to 50 GHz to obtain the y-parameters and were de-embedded with a two step (open and short) procedure. Extrinsic device components such as source/drain resistance and substrate related parameters were extracted and de-embedded. To obtain $R_g$, $\mathrm{Re}(Y_{11})/(\mathrm{Im}(Y_{11}))^2$ is used and it is based on the y-parameter analysis of high frequency MOSFET equivalent circuit [7], [8]

$R_g$ is independent of frequency but is sensitive to bias. Extracted $R_g$ approaches $R_{ele}$ at high $V_{gs}$ because resistance in channel ($R_{ch}$) decreases to zero [7], [8]. Thus, $R_{ele}$ was obtained from $R_g$ measured at high $V_{gs}$ and low $V_{ds}$.

$R_{ele}$ which has multiple-fingers and contacts on both sides of the gate consists of several parts [1]:

$$R_{ele} = \frac{R_{sh}}{12}\frac{W_f}{L \times N_f} + \frac{R_{sh}}{2}\frac{W_{ext}}{L \times N_f} + \frac{1}{2}\frac{R_{via}}{N_{via} \times N_f} + \frac{\rho_{cnt}}{W_f \times L \times N_f} + R_{ext} \quad (1)$$

where $R_{sh}$ is the silicide sheet resistance, $L$ is gate length, $W_f$ is the unit finger width, $W_{ext}$ is extrinsic poly silicide beyond active region, $\rho_{cnt}$ is the specific contact resistivity between silicide and polysilicon layers, $N_f$ is the number of fingers in unit finger, $R_{via}$ is the resistance of a metal1-to-polysilicon via, $N_{via}$ is the number of vias per unit finger, and $R_{ext}$ is external resistance without dependence on $N_f$. The vertical structure through A to B line in Fig. 1(a) is shown in Fig. 1(b) which illustrates $R_{sh}$ and $\rho_{cnt}$.

## 3. Results and discussion

At first, $R_{ele}$ was obtained for different number of fingers ($N_f$ = 16, 30, and 48) when $W_f$ is 0.8 μm, $W_{ext}$ is 0.17 μm, and $N_{via}$ is 1.4. With them, $R_{ext}$ in eq. (1) was extracted because it had no dependence on $N_f$ and the extracted value was 0.01 Ω as shown in Fig. 2. Both $R_{sh}$ and $\rho_{cnt}$ were also obtained by extracting $R_{ele}$ with MOSFETs which has different unit finger width ($W_f$ = 1.6 and 3.2). The values of $R_{sh}$ and $\rho_{cnt}$ were 9.5 Ω/sq and 15.7 Ωμm$^2$ in NMOSFETs, whereas those in PMOSFETs were 10.4 Ω/sq and 28.7 Ωμm$^2$, respectively. Those differences between NMOSFETs and PMOSFETs are mainly due to the difference in the polysilicon doping concentration and silicide profile.

The contact resistivity $\rho_{cnt}$ is high as much as it can not be ignored and depends only on total width and length of device in eq. (1). With the scaling-down of the minimum design rule, the interface resistance between the silicide and the polysilicon layers will be more important in $R_{ele}$ and cannot easily be reduced without alternative gate materials or structures such as metal gates [10].

Similarly, we can understand the $W_f$ dependence of $R_{ele}$ in NMOS in Fig. 3. As $W_f$ decreases, $R_{poly}$ becomes higher because the 4th term ($\rho_{cnt}$) in eq. (1) dominates. As $W_f$ increases, $R_{ele}$ eventually increases because the 1st term ($R_{sh}$) in eq. (1) dominates. The optimum finger width can be obtained by equating the two terms.

$$W_f\big|_{OPT} = \sqrt{12\rho_{cnt}/R_{sh}} \quad (2)$$

In this work, the optimum finger width is 4.5 μm in NMOSFETs whereas it is 5.8 μm in PMOSFETs. The larger optimum finger width of PMOSFETs is mainly due to the higher $\rho_{cnt}$ in PMOSFETs, which comes from smaller doping concentration. For 65nm and 130nm technology with N/PMOSFETs with different $N_f$, the $R_{poly}$ model and

measurement shows a good agreement as shown in Fig. 4. $R_{elec}$ was lower in 130nm technology than in 65nm technology because Co-salicided polysilicon process was used in 130nm while No-salicided polysilicon process was used and there were the differences of materials, silicide thickness and thermal budget. For 130nm technology, $R_{sh}$ and $\rho_{cnt}$ were 3.8 Ω/sq and 2.4 Ωμm$^2$ in NMOSFETs, whereas those in PMOSFETs were 5.0 Ω/sq and 6.1 Ωμm$^2$.

## 4. Conclusion

In this paper, we propose the method of extracting $R_{sh}$ and $\rho_{cnt}$ directly in both n-type and p-type RF MOSFETs without extra patterns or simulations. Also, the gate electrode resistance model is verified with measured values for 65nm and 130nm technology. Optimum gate finger width was obtained using simple equation. The optimum finger width was larger in PMOSFETs than in NMOSFETs.


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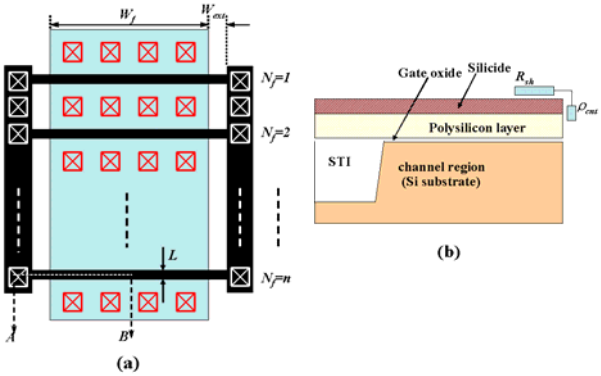


Fig. 1. (a) Schematic layout of multiple-finger, showing and (b) cross section of the polysilicon gate through the line A-B in (a), showing the silicide sheet resistance and silicide-to-polysilicon interface resistivity.

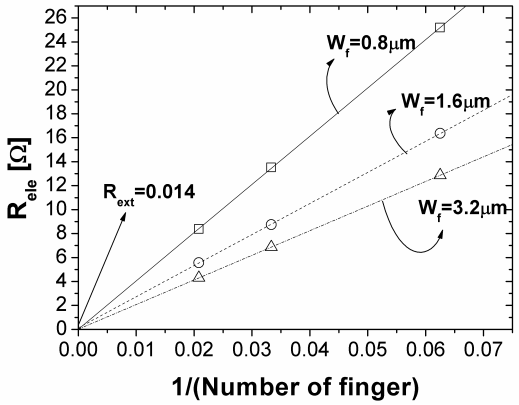


Fig. 2. Extracted value of $R_{ext}$ with varying the number of fingers ($1/N_f$) for different $W_f$.

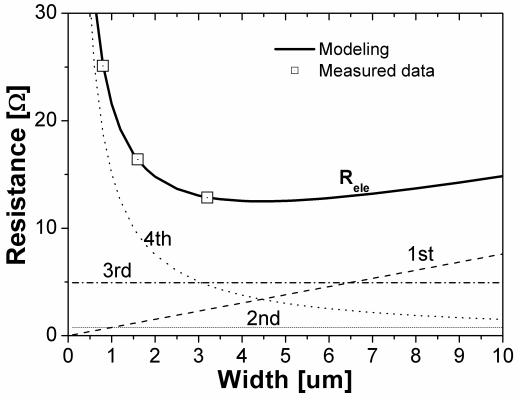


Fig. 3. Curves of $R_{ele}$ versus $W_f$ in 65nm NMOS ($N_f$ =16), which show the value of all components in (1). A significant increase in $R_{ele}$ can be seen with narrower $W_f$ because the 4th term ($\rho_{cnt}$) dominates $R_{ele}$ while $R_{ele}$ with wider $W_f$ also is increased because the 1st term ($R_{sh}$) dominates $R_{ele}$. $W_f$ having the minimum $R_{ele}$ is 4.5 μm in NMOS.

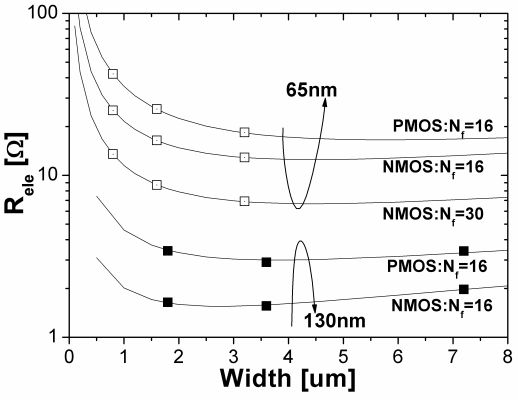


Fig. 4. Curves of $R_{ele}$ versus $W_f$ with varying multiple fingers in both NMOS and PMOS. $W_f$ for 65nm technology has minimum $R_{ele}$ at 4.5 μm in NMOS and 5.8 μm in PMOS, whereas $W_f$ has minimum $R_{ele}$ at 2.8 μm in NMOS and 3.7 μm in PMOS for 130nm technology.