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Mechanism and Reliability Index of Hot-Carrier Degradation in LDMOS Transistors

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1. Introduction

High-voltage lateral DMOS (LDMOS) transistors have been widely used in many smart power applications because of their compatibility with standard low-voltage CMOS process. However, LDMOS transistors are sensitive to hot-carrier degradation because high voltages are applied to the drain and gate. Since the electric field and current distribution in LDMOS devices are a complex function of bias condition and device design, hot-carrier degradation of LDMOS transistors is more complicated than that in low-voltage MOSFETs. Several studies have reported that the behavior of hot-carrier degradation in LDMOS devices is quite different from low-voltage MOSFETs [1]-[4].

In this work, the mechanism of hot-carrier degradation in LDMOS devices is investigated. Electron injection induced interface state (N_{it}) generation in the channel region is identified to be the main degradation mechanism. Furthermore, gate current (I_g) has a good correlation to device degradation, indicating that I_g can be used as a reliability index in our LDMOS devices.

2. Experiments

The schematic cross section of the n-type LDMOS transistor used in this work is shown in Fig. 1. This device is fabricated by a 0.25μm CMOS process with STI for device isolation and features a HV n-well near the drain side. Three important layout parameters: L, b, and S1 correspond to the length of the channel, the length from HV n-well edge to poly-gate edge, and gate-to-drain space are also indicated in the figure. The dimension of devices used in this study is L ≈ 0.5μm, b ≈ 0.7μm, and S1 ≈ 0.4μm. The operational voltage of the device is V_{ds} = V_{gs} = 12V. DC stressing under V_{ds} = 13.2V and V_{gs} = 6V at room temperature was performed. The on-resistance (R_{on}) measured under V_{ds} = 0.1V and V_{gs} = 12V, maximum transconductance (G_{mmax}) and threshold voltage (V_T) extracted under V_{ds} = 0.1V were monitored. Charge pumping measurement [5] was also carried out to evaluate the hot-carrier-induced N_{it} generation. Charge pumping current (I_{cp}) was measured at the bulk while pulsing the gate and grounding the source and drain. The stress tests were interrupted periodically to measure the degradation of device parameters and I_{cp}.

3. Results and Discussion

Fig. 2 shows the measured R_{on}, G_{mmax}, and V_T shift as a function of stress time. The degradation of G_{mmax} is much greater than R_{on} and V_T shift. G_{mmax} degradation is attributed to the decrease in channel mobility caused by interface state generation. On the other hand, V_T shift is the result of charge trapping in the gate oxide and charged interface states in Si/SiO_2 interface in the channel region. Significant G_{mmax} degradation but little V_T shift suggests that hot-carrier-induced damage in this device is mainly neutral interface states in the channel region.

To identify the degradation mechanism, the results of two-dimensional TCAD simulation and charge pumping measurement are analyzed. Fig. 3 shows the vertical electric field along the Si/SiO_2 interface and there is a sign change in vertical electric field between channel and n-well region. Fig. 4 shows the carrier injection probability along the Si/SiO_2 interface, where Lucky Electron model for both electrons and holes are adopted. It is clear that both electron injection and hole injection occur in this device simultaneously, however, the probability of electron injection is six orders of magnitude greater than hole injection. Such a result reveals that device degradation is mainly resulted from electron injection in the channel region. According to data in Fig. 2, it is suggested that the electron injection creates donor-type interface states and those traps are neutral [6], resulting in significant G_{mmax} degradation but little V_T shift. Some R_{on} degradation is also exhibited because drain current decreases as a result of decrease in channel mobility. Fig. 5 shows the R_{on} and G_{mmax} degradation vs. ΔI_{cp}, where ΔI_{cp} is the stress-induced increase in I_{cp}. ΔI_{cp} is highly correlated to both R_{on} and G_{mmax} degradation. Such a result further confirms that device degradation is mainly caused by N_{it} generation.

To verify electron injection in the channel region is the driving force of degradation, devices with various layout parameter b were stressed under the same condition. As seen in Fig. 6, R_{on} degradation decreases as b increases because the electron injection in the channel region is less severe as seen in Fig. 7. Since I_g is mainly resulted from electron injection in the channel, it is suspected that I_g can correlate with device degradation well. Fig. 8 shows the extrapolated lifetime as a function of stressing I_g for devices with various L, b, and S1. The lifetime criterion is defined as 10% of R_{on} degradation. Contrary to the degradation of low-voltage CMOS devices where substrate current is used as an index, I_g correlates well with lifetime in our samples. Such a result indicates that I_g can be used as a reliability index in our LDMOS devices.

4. Conclusions

The hot-carrier reliability and degradation mechanism of high-voltage LDMOS transistors are studied. Experimental data and TCAD simulations indicate that device degradation is mainly caused by electron injection induced N_{it} generation in the channel region. Since I_g is mainly resulted from the electron injection, I_g can be used as a reliability index in our LDMOS devices.

Acknowledgements

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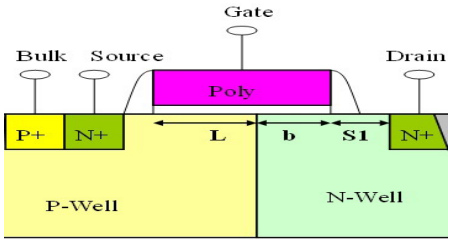

Fig. 1 The schematic cross section of the n-type LDMOS device.

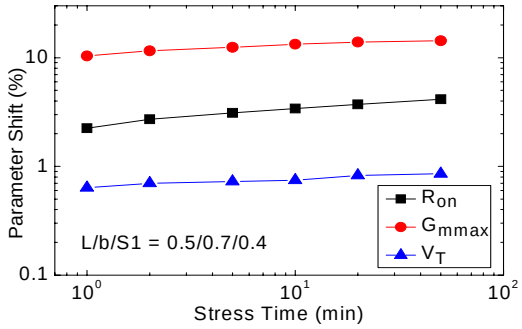

Fig. 2 G_{mmax} degradation is much greater than R_{on} and V_T shift, indicating damage is mainly neutral interface states in the channel.

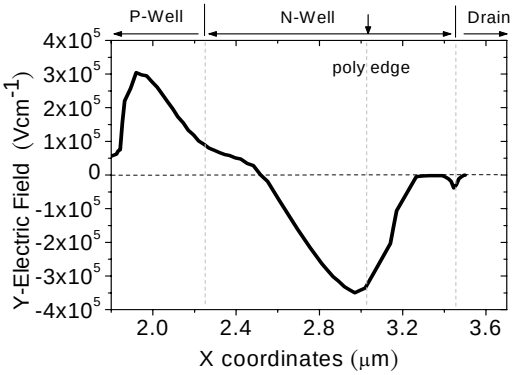

Fig. 3 Vertical electric field along the Si/SiO_2 interface. There is a sign change between channel and n-well region.

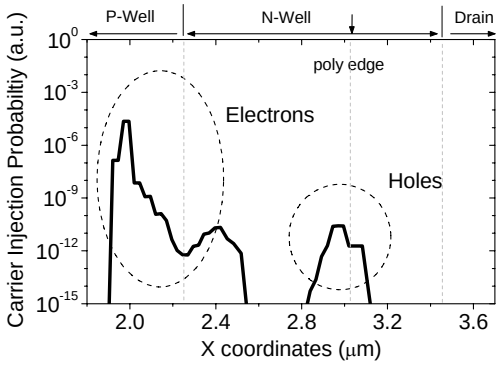

Fig. 4 Hot carrier injection probability along the Si/SiO_2 interface. Electron injection in the channel is significant.

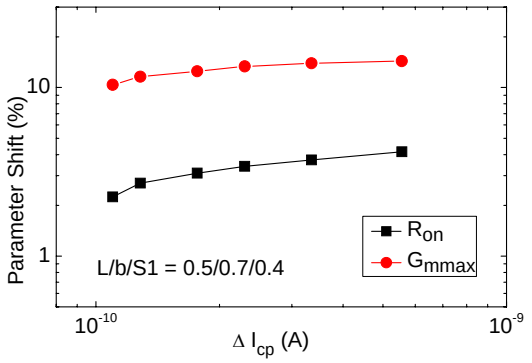

Fig. 5 ΔI_{cp} is highly correlated to R_{on} and G_{mmax} degradation, indicating that degradation is mainly caused by N_{it} generation.

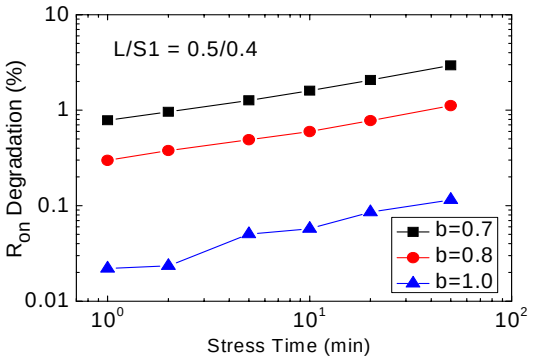

Fig. 6 R_{on} degradation becomes smaller with increasing layout parameter b.

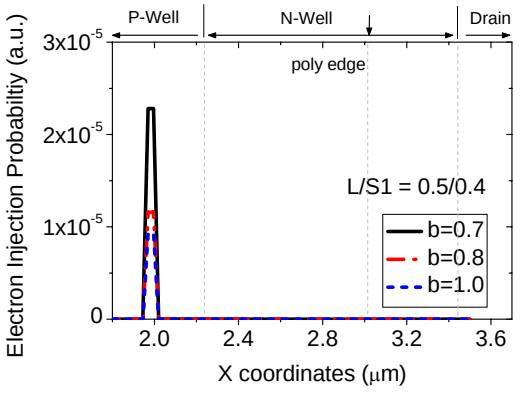

Fig. 7 The electron injection probability becomes less when layout parameter b is larger.

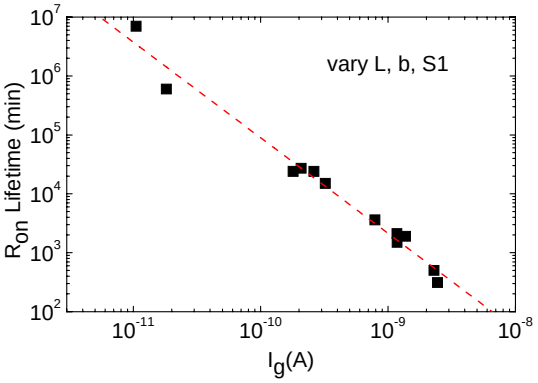

Fig. 8 I_g correlates well with R_{on} lifetime, indicating that I_g can be used as a reliability index.