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Anomalous Hot-Carrier-Induced On-Resistance Degradation in High-Voltage LDMOS Transistors

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1. Introduction

To fulfill the trend of lower cost and smaller chip size, high-voltage MOS devices have been widely used in smart power management IC and flat panel display drivers. Lateral diffused MOS (LDMOS) transistors attracted most attention among the various types of high-voltage devices because they can be easily implemented into the standard CMOS process flow [1]-[2]. One major reliability issue of the LDMOS transistors is the hot-carrier reliability due to their high operating drain and gate voltages.

In this work, hot-carrier reliability of 12V n-type LDMOS transistors is investigated. It has been reported that LDMOS transistors with significant Kirk effect produce much greater on-resistance (R_{on}) degradation at high V_g bias than at the V_g bias corresponding to the first $I_{b(peak)}$ [3]-[4]. However, our data indicate that R_{on} degradation is similar at medium to high V_g bias, though I_b is much larger at high V_g bias. Based on experimental data and two-dimensional TCAD simulation, the mechanism responsible for this anomalous R_{on} degradation will be discussed.

2. Experiments

The schematic cross section of the n-type LDMOS device used in this work is shown in Fig. 1. The fabrication of this device is modified from a standard 0.35μm CMOS process flow. The length of poly-gate, channel region, and the overlap between gate and NDD region are 0.8μm, 0.25μm, and 0.25μm, respectively. The operating voltage is 12V for both V_d and V_g. DC stressing with various V_g and V_d = 13.2V under room temperature was carried out with the source and body connected to the ground. Charge pumping measurement similar to the method in [4] was also performed to quantify the interface state generation (ΔN_{it}) during stressing. The pulse with high level fixed at 1.6V and variable amplitudes was applied to the gate under a frequency of 500 kHz. The maximum of transconductance ($G_{m(max)}$) and V_T measured at V_d = 0.1V, and R_{on} (=V_d/I_d) measured at V_d = 0.1V, V_g = 12V were monitored. The stressing experiments were interrupted periodically to measure the degradation of device parameters and ΔN_{it}.

3. Results and Discussion

Fig. 2 shows the R_{on} and $G_{m(max)}$ degradation stressed under V_d = 13.2V, and V_g = 6V for 50 min. The V_T shift is little (< 5mV) and not shown in the figure. R_{on} degrades much greater than $G_{m(max)}$ revealing that hot-carrier induced damage is mainly located in the NDD drift region [5]. The I_b-V_g characteristics is shown in Fig. 3 and I_b increases monotonously with V_g. This trend is different from some LDMOS devices where two peaks of I_b-V_g characteristics is exhibited. Our data indicate that the occurrence of Kirk effect in our device is as early as medium V_g bias due to a low dosage in the NDD drift region [6]. Fig. 4 shows the R_{on} degradation under various stressing V_g at V_d = 13.2V. R_{on} degradation is much smaller under low stressing V_g (V_g = 3V). Such a result is expected because I_b is much smaller under low V_g as in Fig. 3. However, R_{on} degradation is almost identical at medium (V_g = 6V) to high stressing V_g (V_g = 9V) even though I_b is much larger at high V_g bias.

To investigate the degradation mechanism under different stressing V_g, N_{it} formation in different regions were analyzed. TCAD simulation was carried out to extract the flat-band voltage and V_T in three regions (channel, HVNW, and NDD). Then ΔN_{it} in different regions can be extracted using the method in [7]. Fig. 5 shows ΔN_{it} in the HVNW region and the amount of ΔN_{it} is similar under different stressing V_g. Fig. 6 shows ΔN_{it} in the NDD drift region. From Fig. 5 and Fig. 6, R_{on} degradation is mainly attributed to ΔN_{it} in the NDD drift region rather than in the HVNW region because of the following two reasons. First, ΔN_{it} in the NDD drift region is roughly 20 times greater than ΔN_{it} in the HVNW region. Second, ΔN_{it} in NDD drift region is smaller at stressing V_g = 3V, however, ΔN_{it} at stressing V_g = 6V and 9V is similar. Such a trend is consistent with the R_{on} degradation data shown in Fig. 4.

To explain the similar R_{on} degradation between stressing V_g = 6V and 9V, impact ionization rate at various V_g and V_d = 13.2V was simulated and shown in Fig. 7. Higher V_g bias produces a greater impact ionization rate, in consistent with the I_b data in Fig. 3. The vertical electric field (E_y) along Si/SiO_2 interface is analyzed in Fig. 8. Under V_g = 3V and 6V, the direction of E_y in the NDD drift region is pointing upward to the Si/SiO_2 interface, which favors hole injection. On the other hand, the direction of E_y is pointing downward to the Si/SiO_2 interface, which favors electron injection when V_g = 9V. According to Fig. 8, ΔN_{it} under V_g = 6V is caused by hole injection, however, ΔN_{it} under V_g = 9V is the result of electron injection. It has been reported that hole has much higher efficiency to create N_{it} than electron does [8]. Stressing at V_g = 6V has higher N_{it} generation efficiency than stressing at V_g = 9V. Since stressing at V_g = 6V has less impact ionization rate than stressing at V_g = 9V, it is suggested that the similar R_{on} degradation between stressing V_g = 6V and 9V is the result of two combined factors: impact ionization rate and N_{it} generation efficiency. Although E_y also favors hole injection at V_g = 3V, the impact ionization rate is much smaller and deeper from the interface, leading to little R_{on} degradation when stressing at V_g = 3V.

4. Conclusions

The hot-carrier reliability of LDMOS transistors is investigated. R_{on} degradation is mainly resulted from N_{it} generation in NDD drift region. Further, R_{on} degradation is not well correlated with I_b. Such an anomalous R_{on} degradation is suggested to be the result of two combined factors: impact ionization rate and N_{it} generation efficiency.

Acknowledgements

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References

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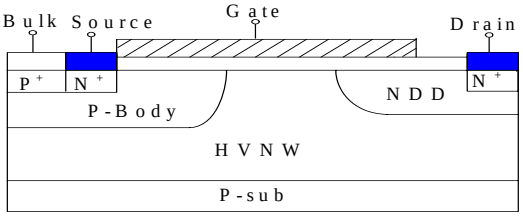

Fig. 1 The structure of the LDMOS transistor used in this work.

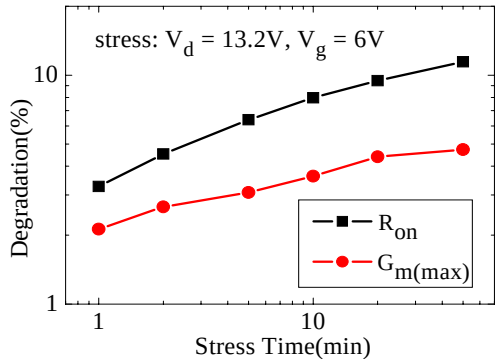

Fig. 2 R_{on} degradation is much greater than $G_{m(max)}$ degradation, revealing that hot-carrier induced damage is mainly located in the NDD drift region.

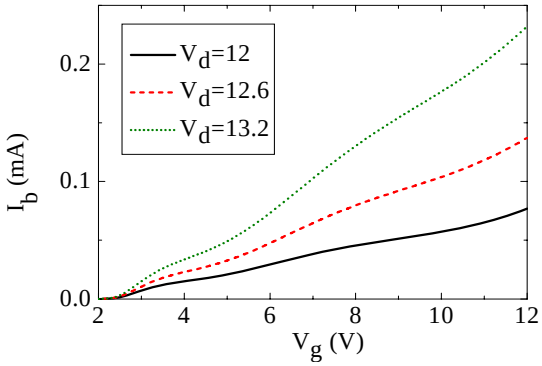

Fig. 3 I_b increases monotonously with V_g.

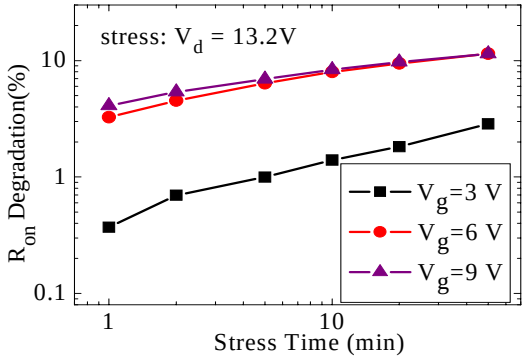

Fig. 4 R_{on} degradation is little at stressing V_g = 3V. However, R_{on} degradation at stressing V_g = 6V and 9V is almost identical.

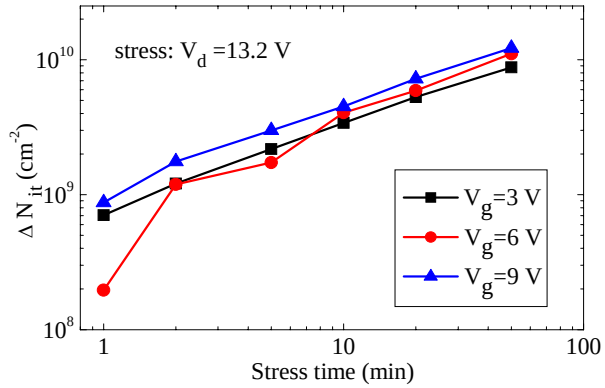

Fig. 5 In the HVNW region, ΔN_{it} is similar under different stressing V_g.

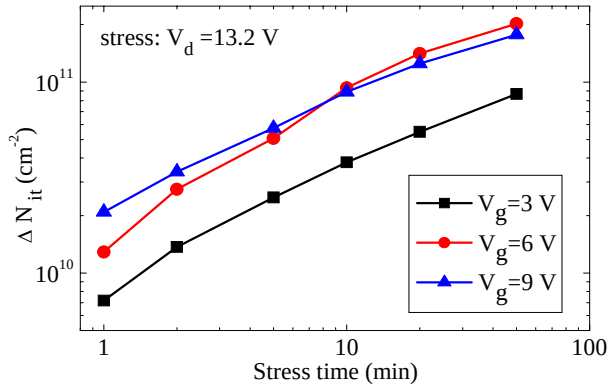

Fig. 6 In the NDD region, ΔN_{it} is smaller at stressing V_g = 3V. However, ΔN_{it} at stressing V_g = 6V and 9V is similar.

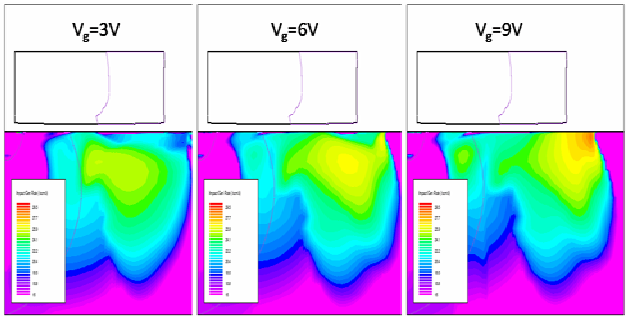

Fig. 7 Impact ionization rate increases dramatically with increasing V_g bias. This is consistent with I_b data in Fig. 3.

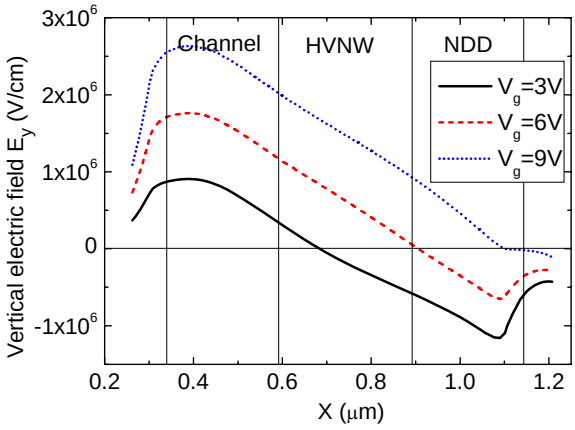

Fig. 8 In the NDD region, E_y favors hole injection at V_g = 3V and V_g = 6V. However, E_y favors electron injection at V_g = 9V.