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Analysis of Temperature Effects on the High-Frequency Characteristics of RF LDMOS Transistors

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1. Introduction

LDMOS transistor technology has played a predominant role in wireless base-station applications for frequencies ranging from 450 MHz to 2.7 GHz, due to its advantages in performance, cost, reliability, and power capability [1]. For high power applications, temperature is an important issue. Several researchers have investigated the influence of temperature on the reliability and dc performance of LDMOS transistors [2-4]. However, the temperature effects on the high-frequency characteristics of LDMOS were seldom addressed. In this paper, the high-frequency characteristics of LDMOS with different layout structures are studied at various temperatures. Some electrical parameters have been extracted to describe the temperature behavior of transistors.

2. Experiments

The device structure of the RF LDMOS used in this work is shown in Fig. 1. The gate oxide thickness was 13.5 nm. We developed two types of layout structures, fishbone and ring, with the same total channel width 360µm (see Fig. 2). For fishbone structure, each cell had 6 fingers with finger width L_F=10µm. For ring structure, the width of each ring was 4×10µm.

3. Results and Discussion

DC characteristics of the LDMOS with different layout structures at -25°C and 50°C are compared in Fig. 3. At low gate voltages (V_{GS}<1V), the transconductance (g_m) and drain current at 50°C are higher than that at -25°C due to the reduction of threshold voltage. At high gate voltages, because the channel mobility decreases with increasing temperature, the g_m and drain current at 50°C become lower than that at -25°C. Fig. 4 shows the extracted drain-source on-resistance (R_{ON}) plotted against the temperature at V_{GS}=2 V. The R_{ON} is lower in the ring structure and increases with increasing temperature due to the reduction of carrier mobility in the channel and drift regions.

The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) versus the gate voltage for LDMOS with different layout structures at various temperatures are shown in Fig. 5. Both f_T and f_{max} decrease with increasing temperature. The degradations of f_T and f_{max} are attributed to the lower intrinsic transconductance as shown in Fig. 6. The variation of both f_T and intrinsic g_m are 22% approximately at V_{GS}=2V, as temperature changes from -25°C to 50°C. Because the temperature dependence of f_{max} is also affected by the drain resistance (R_d) and drain-substrate junction capacitance (C_{jdb}), the variation of f_{max} is 18% approximately. It should be noted that the f_T and g_m have a zero-temperature-coefficient bias point near V_{GS}=1V. The zero-temperature-coefficient bias point is resulted from the negative temperature coefficients of both the effective mobility and threshold voltage [3].

Figure 7 shows the measured *S*-parameters of the fishbone and ring structures at various temperatures. The transistors were measured at V_{GS}=2V and drain voltage V_{DS}=28V for the maximum value of f_T. As shown in Fig. 7, the deviation of *S*11 is not obvious with temperature. It suggests that the input impedance is affected by temperature slightly. The *S*12 has minor change at low frequency. However, the kink phenomenon in *S*12 will occur at high temperatures, making obvious deviation of *S*12 with temperature as the frequency is higher than the kink point. Because the g_m decreases with increasing temperature, both *S*21 and *S*22 changes significantly. It is interesting that the temperature-induced variation of *S*22 in the ring structure is lower than that in the fishbone structure. The extracted R_d and C_{jdb} of the ring structure are 7.8Ω and 149fF, respectively, which are lower than that of the fishbone structure (The extracted R_d and C_{jdb} are 18Ω and 244fF, respectively) [5]. This is a possible reason for the lower *S*22 variation of ring structure with different temperatures.

4. Conclusions

The temperature effects on the high-frequency characteristics of RF LDMOS transistors are investigated. The degradations of f_T and f_{max} at high temperatures are due to the reduction of transconductance. In addition, the temperature dependence of f_{max} will also be affected by the drain resistance and drain-substrate junction capacitance. The *S*-parameters at various temperatures are also discussed. Because the LDMOS transistors with ring structure have lower drain resistance and drain-substrate junction capacitance, the variation of *S*22 with temperature is smaller than that of fishbone structure.

References

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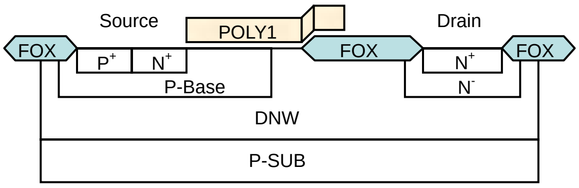

Fig. 1. Cross-section of an LDMOS transistor.

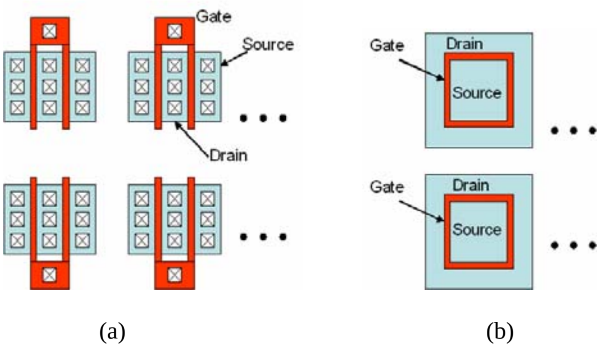

Fig. 2. LDMOS layout structures: (a) fishbone. (b) ring.

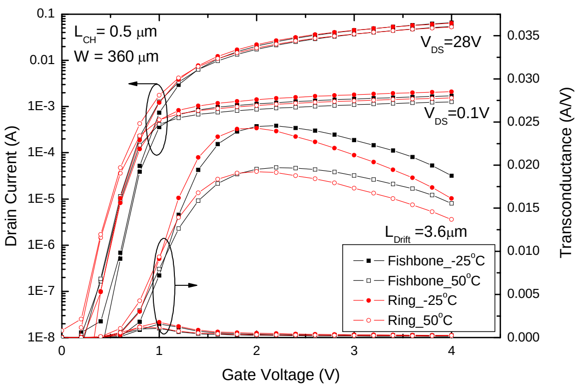

Fig. 3. Drain current versus gate voltage for LDMOS transistors with different structures and different temperatures.

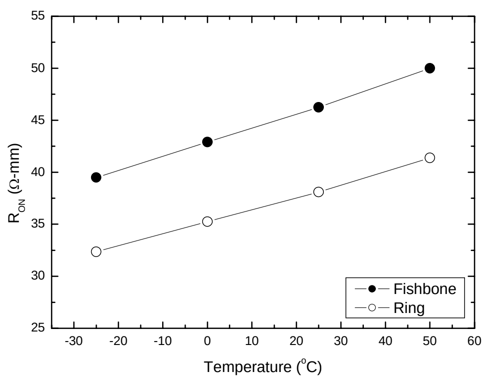

Fig. 4. R_{ON} versus temperature for different layout structures.

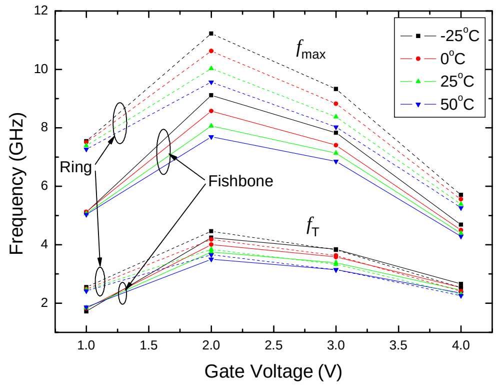

Fig. 5. Cut-off frequency and maximum oscillation frequency versus gate voltage at various temperatures.

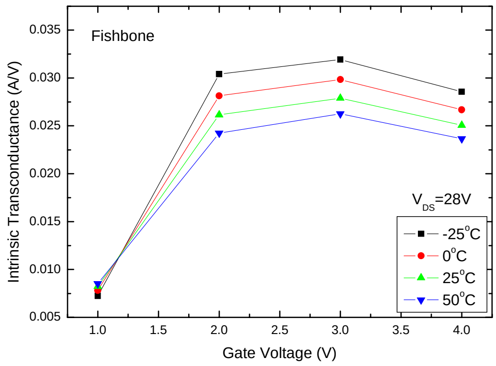

Fig. 6. Extracted intrinsic transconductance versus gate voltage at various temperatures.

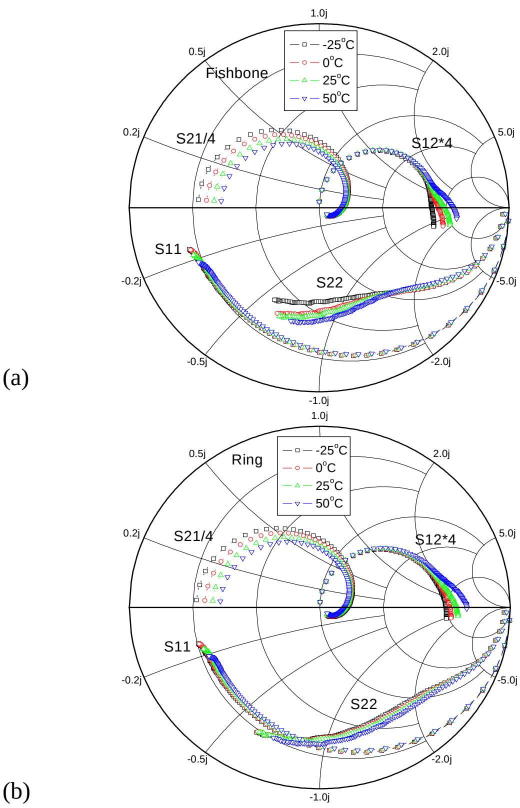

Fig. 7. Measured *S*-parameters of transistors with (a) fishbone and (b) ring structures from 0.1GHz to 20 GHz.