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Cross-Current SOI MOSFET Model and Important Aspects of CMOS Operations

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I. INTRODUCTION

One of the authors (Omura) proposed the cross-current tetrode SOI MOSFET (XCT-SOI MOSFET) to examine analog applications (see Fig. 1) [1]. Though scaling feasibility of XCT-like devices has been studied recently [2], we think XCT devices will yield new applications such as high-voltage devices and SRAM memory cells with high noise margin. In order to discuss those applications in sufficient detail device models are needed to perform circuit simulations. However, modeling an XCT device is not so easy because of the three-dimensionality of its operations.

This paper proposes a quasi-3D device model for the XCT SOI MOSFET that allows its various aspects to be considered. Here we make a depletion approximation and simplify the potential coupling effects of MOSFET and JFET.

II. DEVICE STRUCTURE AND ASSUMPTIONS FOR MODELING

A. Device structure and features

Schematic device structure is shown in Fig. 1. In an XCT device, the n-channel MOSFET and p-channel JFET are self-merged and the electron current of nMOSFET is relayed to the hole current of pJFET in series. The XCT device offers negative differential conductance in the saturation region of drain current [1]. Since the XCT device has active body contact, from pJFET, the body-floating effect is eliminated automatically.

B. Assumptions for modeling

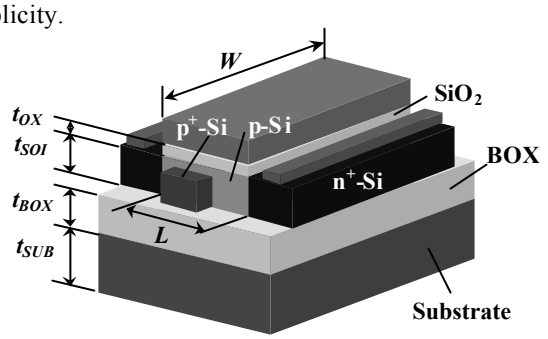
In modeling the drain current, we must take account of the potential coupling effect between nMOSFET and parasitic pJFET because the local potential (f) of the p-type body of pJFET works as an effective reverse body bias structure of nMOSFET; as shown in Fig. 1, source and drain depletion layer widths (W_S and W_D) vary from one p^+ body contact (the source of pJFET) to the other (the drain of pJFET) because the p-type body potential varies from one p^+ body contact to the other. MOSFET channel current is expressed as

$$I_{MOSFET} = \int_0^W \frac{m_n}{L}\left[C_{ox}\left\{V_G - V_{FB} - f_s - \frac{1}{2}(V_D + V_o)\right\}(V_D - V_o) - \frac{2}{3}\sqrt{2e_S q N_A}\left\{(f_s + V_D - j(y))^{3/2} - (f_s + V_o - j(y))^{3/2}\right\}\right] dy, \quad (1)$$

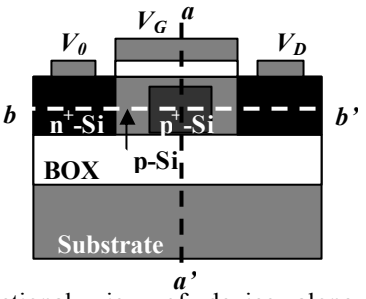
where V_O is the source potential of the MOSFET and $j(y)$ is the body potential of p-type region. Other notations have their conventional meanings. On the other hand, the channel current of JFET is expressed as

$$I_{JFET} = qN_A m_p \left(\frac{\partial j}{\partial y}\right)\{L - a(W_S + W_D)\}\{t_{SOI} - W_{CH}\}, \quad (2)$$

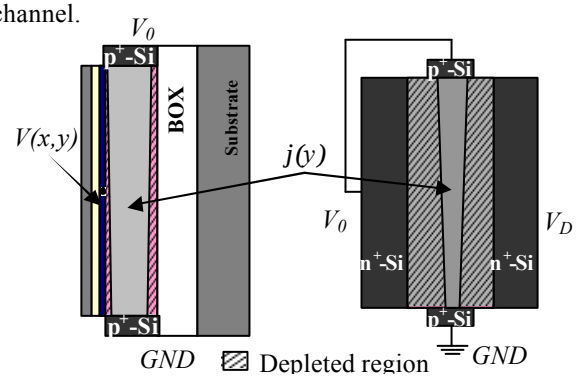
where W_S, W_D and W_{CH} are the source, the drain and the channel depletion layers, respectively. t_{SOI} is the SOI layer thickness and α is the fitting parameter to adjust the expansion of depletion layers. Here, to formulate the channel current, we introduce the depletion approximation and gradual-channel approximation for simplicity [3]. In the present model, the channel cross-section of JFET excludes the depletion region on the buried oxide for simplicity.



(a) Bird's eye view of XCT device with parameter definitions.



(b) Cross-sectional view of device along MOSFET channel.



(c) Cross-sectional view of device along a-a' and b-b'.

Fig. 1. XCT SOI MOSFET (bird's eye view and cross-sectional views)

C. Derivation of model equations

Using current continuity, the derivative of body potential can be formulated as

$$\frac{\partial j}{\partial y} = \frac{-\frac{2}{3}KP_{DB}^{3/2} - \frac{2}{3}KP_{0B}^{3/2} + \frac{2}{3}KP_{DB0}^{3/2} + \frac{2}{3}Kf_B^{3/2} + LV_0}{W\{K(V_D + f_B - j)^{1/2} + K(V_0 + f_B - j)^{1/2} - L\}}, \quad (3)$$

$$P_{0B} = (V_0 + f_B), \quad (4)$$

$$P_{DB} = (V_D + f_B), \quad (5)$$

$$P_{DB0} = (V_D + f_B - V_0), \quad (6)$$

where K is the device-parameter-dependent constant [3]. Next, equation (1) is integrated and equation (2) is solved.

III. EXPERIMENTAL RESULTS OF SOI MOSFET AND XCT DEVICES

A. *Experimental results of fabricated devices*

First, we show the fundamental I_D-V_D characteristics of an nXCT device in Fig. 2. Device parameters of the fabricated device are summarized in Table I. It is seen that I_D of the XCT device is lower than that of the original MOSFET [4] because of the series resistance of the parasitic pJFET. On the other hand, the short-channel effects of the original MOSFET are only slightly reproduced in the XCT device, which is an important feature of XCT devices. Simulations of the XCT device successfully reproduce the experimental results including negative differential conductance (NDC) in the saturation region [1], which indicates validity of the proposed model.

Table. 1. Device parameters assumed in I_D-V_D

Device parameters	Values	[units]
Nominal body doping*, N_A	9×10^{14}	[cm^{-3}]
Gate width, W	10	[μm]
Gate length, L	2	[μm]
Gate oxide thickness, t_{ox}	30	[nm]
SOI layer thickness, t_{SOI}	350	[nm]

Physical parameters for calculations	Values	[units]
Electron mobility for MOSFET	600	[cm^2/Vs]
Hole mobility for JFET	450	[cm^2/Vs]
Built-in potential, ϕ_B	0.9	[V]

* N_A of 1×10^{16} cm^{-3} is assumed in calculations by taking

IV. XCT-CMOS CHARACTERISTICS

The XCT-CMOS should offer low power consumption because its drain current level is lower than that of the original MOSFET as already described. In addition, we wish to pay attention to the suppression of short-channel effects as shown in Fig. 2. This suggests that the XCT-CMOS would show better transition characteristics and a high noise margin. We show transition characteristics of XCT-CMOS in Fig. 3.

Fig. 3 shows that the XCT-CMOS offers a sharp transition, and that the logic threshold is almost independent of the supply voltage, which is the most important feature of the XCT-CMOS structure. In the conventional CMOS, pMOS and nMOS have threshold voltages of –0.60 V and +0.60 V, respectively. The equivalent values for the pXCT device and nXCT device are -0.49 V and +0.49 V, because of the effective positive body bias for the pXCT device and the negative body bias for the nXCT device. The body bias suppresses short-channel effects and improves the noise margin.

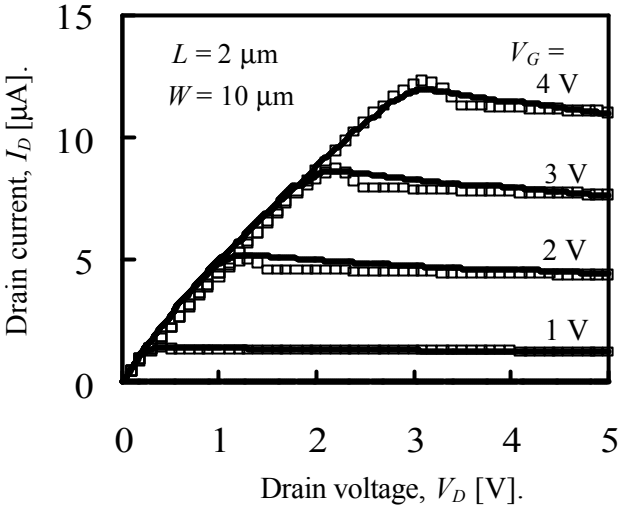


Fig. 2. I_D-V_D characteristics of XCT device. Calculation results are also shown for comparison.

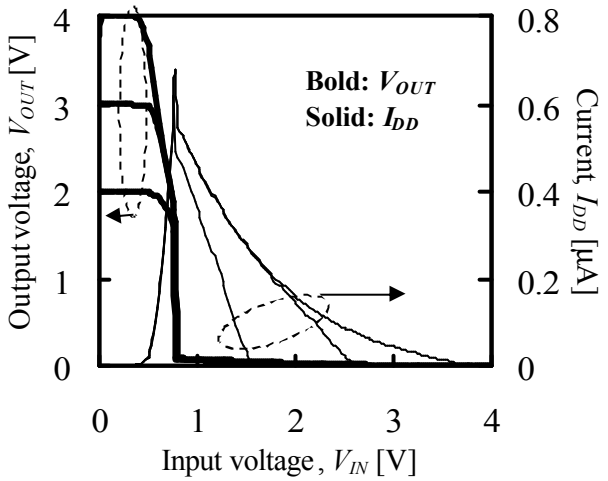


Fig. 3. CMOS transition characteristics (L_n=L_p= 2 μm, W_n=W_p= 10 μm)

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