Performance Comparison of Ultra-thin FD-SOI Inversion-, Intrinsic- and Accumulation-Mode MOSFETs

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INTRODUCTION

Ultra-thin SOI devices have been recognized as an alternative device structure to the bulk CMOS devices due to the several advantageous characteristics such as lower leakage current, better short channel immunity and less parasitic capacitance [1]. To maximize the usability of the device, this work demonstrates the device simulation based performance comparison of ultra-thin FD-SOI Inversion-, Intrinsic and Accumulation-Mode MOSFETs in terms of their current drivability and subthreshold scalability for various gate length (Lg), SOI layer thickness (tSOI) and wide range of SOI dopant concentration (NSOI). In addition, performance comparison is extended to the poly-Si gate electrode process for Accumulation-Mode and Inversion-Mode MOSFETs with regards to the poly-depletion effect.

SIMULATION CONDITIONS

Simulation condition in the first part of this work assumes that workfunction of the gate electrode metal is tunable. In this work, the mobility model that depends on the impurity concentration and temperature is used for low electric field region [4], as well as the universal mobility relationship for Si(100) surface orientation is used for the inversion and accumulation layers [5]. Saturation velocity for electron is set to 1.0x10^7 cm/sec. Contact resistance at inversion and accumulation layers [5]. Saturation velocity relationship for Si(100) surface orientation is used for the electric field region [4], as well as the universal mobility the impurity concentration and temperature is used for low

A. Effect of SOI layer dopant concentration and types

Firstly, subthreshold scalability is analyzed with regards to the NSOI and tSOI. Figs. 2 (a-c) show the threshold voltage roll off characteristics from a long channel devices at Vds=1 V for various NSOI and tSOI, respectively. The results show that subthreshold scalability is better for Inversion-, Intrinsic- and Accumulation-Mode MOSFETs, in that order for thicker tSOI. However for thin tSOI such as below 10 nm, the subthreshold scalabilities are better for thinner tSOI and become comparable for various dopant concentrations for both impurity types [6].

The results suggest that Accumulation-Mode MOSFETs would realize higher current drivability than Inversion- or Undoped- (Intrinsic) MOSFETs. Also, Accumulation-Mode MOSFETs would extend the poly-Si gate electrode LSI manufacturing processes even for very short channel generation with a sufficient Vth control because the problems due to the poly-Si depletion do not arise.

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REFERENCES

Fig. 1 Schematic of the FD-SOI MOSFET structure for the simulation [6]. Silicon channel region is doped with, n-type impurity for Accumulation-Mode, p-type impurity for Inversion-Mode and undoped for Intrinsic-Mode nMOSFETs. Gate electrode would be p-poly-Si for Accumulation-Mode, and n-poly-Si for Inversion-Mode nMOSFETs later in this work.

Fig. 2 High drain voltage $V_{th}$ roll-off characteristics for Inversion-, Intrinsic- and Accumulation-Mode FD-SOI nMOSFETs as functions of gate length. $t_{SOI}$ are 20 nm for (a), 10 nm for (b) and 5 nm for (c), respectively. Subthreshold scalabilities become comparable for various Si channel doping conditions as $t_{SOI}$ becomes thinner.

Fig. 3 (a) Electric filed intensity across the insulator ($E_i$) and (b) electric field intensity in Si at the interface ($E_{Si}$) as functions of gate voltage. Electric filed intensities are supressed for Inversion-, Intrinsic- and Accumulation-Mode MOSFETs in that order at a same $V_{gs}$.

Fig. 4 Saturation drain current ($I_{dsat}$) at $V_{gs}=1.0$ V when $E_i$ is at 6.0 MV/cm for various Si channel doping conditions as functions of $t_{SOI}$. The result shows that Accumulation-Mode MOSFETs can gain the current drivability for a same $t_{SOI}$.

Fig. 5 Gate to channel capacitance ($C_{gch}$) as functions of gate overdrive voltage for Accumulation- and Inversion-Mode nMOSFETs with poly-Si gate electrode of which impurity concentration is varied from $1\times10^{10}$ to $1\times10^{20}$ cm$^{-3}$, respectively. The poly-depletion effect does not occur for the Accumulation-Mode MOSFETs.

Fig. 6 $I_{dsat}-V_{gs}$ characteristics of (a) Accumulation-Mode nMOSFETs and (b) Inversion-Mode nMOSFETs with poly-Si gate electrode of which impurity concentration is varied from $1\times10^{10}$ to $1\times10^{20}$ cm$^{-3}$, respectively. $L_{gate}=30$ nm. Accumulation-Mode MOSFETs maintain the high current drivability even when Np-poly-Si is $1\times10^{19}$ cm$^{-3}$.