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Performance Comparison of Ultra-thin FD-SOI Inversion-, Intrinsic- and Accumulation-Mode MOSFETs

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INTRODUCTION

Ultra-thin SOI devices have been recognized as an alternative device structure to the bulk CMOS devices due to the several advantageous characteristics such as lower leakage current, better short channel immunity and less parasitic capacitance [1]. To maximize the usability of the device, this work demonstrates the device simulation based performance comparison of ultra-thin FD-SOI Inversion-, Intrinsic and Accumulation-Mode MOSFETs in terms of their current drivability and subthreshold scalability for various gate length (L_{gate}), SOI layer thickness (t_{SOI}) and wide range of SOI dopant concentration (N_{SOI}). In addition, performance comparison is extended to the poly-Si gate electrode process for Accumulation-Mod and Inversion-Mode MOSFETs with regards to the poly-depletion effect.

SIMULATION CONDITIONS

Fig. 1 shows the schematic view of the device structure used in this work. Dopant profiles of Source and Drain are abrupt to the channel region. In this work, Inversion-, Intrinsic- and Accumulation-Mode MOSFETs are defined as follows.

Inversion-: SOI layer is doped with the opposite impurity type from Source/Drain regions.
Intrinsic-: SOI layer is undoped.
Accumulation-: SOI layer is doped with the same impurity type as Source/Drain regions [2-3].

Simulation condition in the first part of this work assumes that workfunction of the gate electrode metal is tunable. In this work, the mobility model that depends on the impurity concentration and temperature is used for low electric field region [4], as well as the universal mobility relationship for Si(100) surface orientation is used for the inversion and accumulation layers [5]. Saturation velocity for electron is set to 1.0×10^7 cm/sec. Contact resistance at Source and Drain terminals are neglected to focus this study on the comparison of the intrinsic device performances. A 2D device simulator: ATLAS is used for the simulation.

RESULTS AND DISCUSSIONS

A. Effect of SOI layer dopant concentration and types

Firstly, subthreshold scalability is analyzed with regards to the N_{SOI} and t_{SOI}. Figs. 2 (a-c) show the threshold voltage roll off characteristics from a long channel devices at V_{ds}=1 V for various N_{SOI} and t_{SOI}, respectively. The results show that subthreshold scalability is better for Inversion-, Intrinsic- and Accumulation-Mode MOSFETs, in that order for thicker t_{SOI}. However for thin t_{SOI} such as below 10 nm, the subthreshold scalabilities are better for thinner t_{SOI} and become comparable for various dopant concentrations for both impurity types [6].

Figs. 3 (a-b) show the electric field intensity in the gate insulator (E_i) and in Silicon at the front interface (E_{eff}) as functions of gate voltage (V_{gs}) for Inversion-, Intrinsic- and Accumulation-Mode nMOSFETs. The result shows that the E_i and E_{eff} are smaller for Accumulation-, Intrinsic- and Inversion-Mode MOSFETs in that orders for a given V_{gs}. This result indicates that if a same gate overdrive voltage is applied, immunities to reliability issues that relate to the E_i, such as bias and temperature instability and time dependent dielectric breakdown, would be improved for Accumulation-Mode MOSFETs compared to Intrinsic- or Inversion-Mode MOSFETs. Moreover, Drain current drivability is improved for Accumulation-Mode MOSFETs if a same E_i is allowed for these devices. Fig. 4 shows the saturation drain current (I_{dsat}) as function of t_{SOI} for various dopant conditions when the allowable E_i is set to 6.0 MV/cm. I_{dsat} is improved for Accumulation-Mode MOSFETs especially when t_{SOI} is thick. Therefore, by optimizing the t_{SOI} and N_{SOI} for Accumulation-Mode MOSFETs, performance of ultra-thin FD-SOI can be maximized with maintaining the subthreshold scalability.

B. Implementation to the poly-Si gate electrode process

Poly-Si gate electrode device structure is introduced to compare the device performance for the further scaling with the conventional poly-Si gate electrode process including the consideration of poly-Si depletion effect. Inversion- and Accumulation-Mode nMOSFETs are structured as follows. n+-poly-Si is used for the gate electrode of the Inversion-Mode nMOSFET, and p+-poly-Si is used for the gate electrode of the Accumulation-Mode nMOSFET. Fig. 5 shows the Gate to channel capacitance (C_{gc}) for Inversion- and Accumulation-Mode nMOSFETs as function of gate overdrive voltage with two poly-Si impurity concentrations (N_{poly}), 1×10^{19} and 1×10^{20} cm^{-3}, respectively. The result shows that C_{gc} do not decrease for the Accumulation-Mode nMOSFETs even when $N_{poly}=1 \times 10^{19}$ cm^{-3}. However for the Inversion-Mode nMOSFET, C_{gc} significantly decreases. It is because that since p^+-poly-Si is used for the Accumulation-Mode nMOSFET, poly depletion effect does not occur in the Accumulation-Mode MOSFETs. Fig. 6 shows the simulated I_{ds}-V_{ds} characteristics for the Inversion- and Accumulation-Mode nMOSFETs when L_{gate} is 30 nm for the two impurity concentrations of the poly-Si gate electrodes. The results clearly show the advantage of the Accumulation-Mode MOSFETs for the poly-Si gate process for short channel ultra-thin FD-SOI MOSFETs.

CONCLUSION

This work demonstrates the performance comparison of ultra-thin FD-SOI MOSFETs with various SOI layer dopant concentrations given by both impurity types. The results suggest that Accumulation-Mode MOSFETs would realize higher current drivability than Inversion- or Undoped- (Intrinsic) MOSFETs. Also, Accumulation-Mode MOSFETs would extend the poly-Si gate electrode LSI manufacturing processes even for very short channel generation with a sufficient V_{th} control because the problems due to the poly-Si depletion do not arise.

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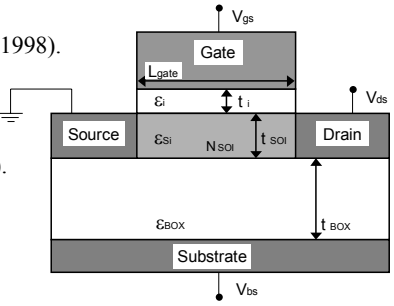

Fig. 1 Sehcmatic of the FD-SOI MOSFET structure for the simulation [6]. Silicon channel region is doped with, n-type impurity for Accumulation-Mode, p-type impurity for Inversion-Mode and undoped for Intrinsic-Mode nMOSFETs. Gate electrode would be p^+-poly-Si for Accumulation-Mode, and n^+-poly-Si for Inversion-Mode nMOSFETs later in this work.

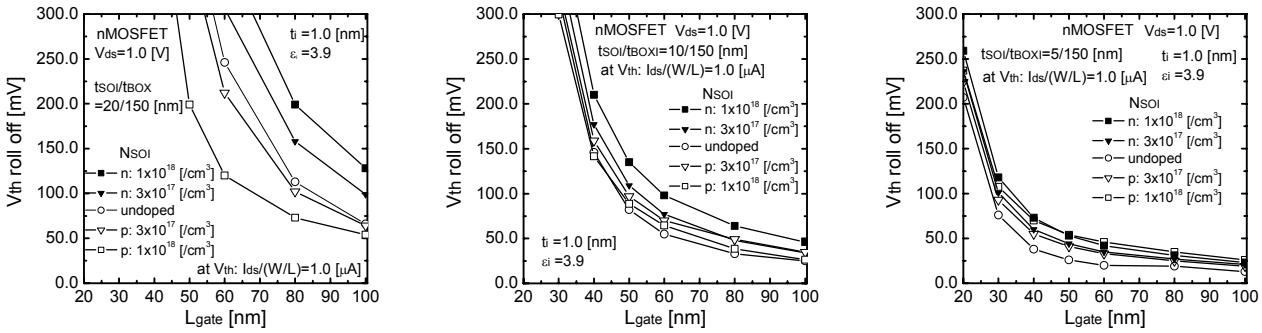

Fig. 2 High drain voltage V_{th} roll-off characterisitics for Inversion-, Intrinsic- and Accumualtion-Mode FD-SOI nMOSFETs as functions of gate length. t_{SOI} are 20 nm for (a), 10 nm for (b) and 5 nm for (c), respectively. Subthreshold scalabilities become comparable for various Si channel doping conditions as t_{SOI} becomes thinner.

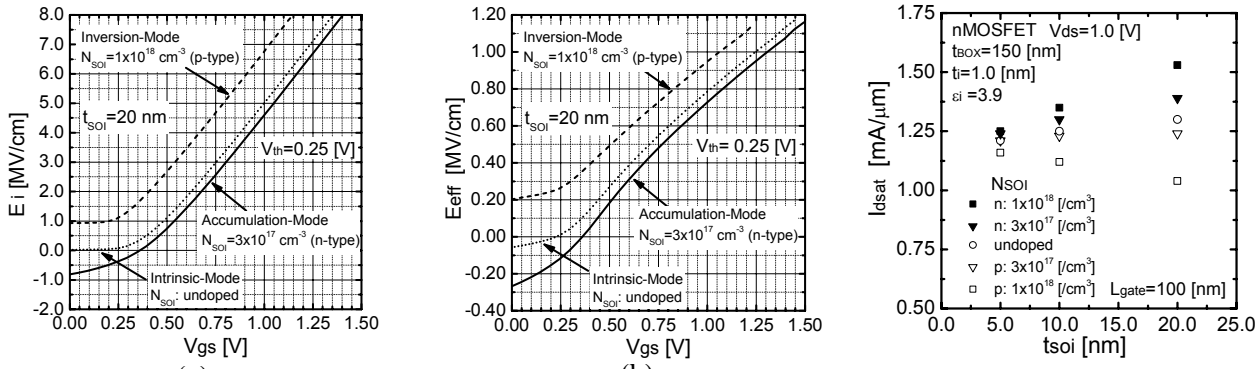

Fig. 3 (a) Electric filed intensity across the insulator (E_i) and (b) electric field intensity in Si at the interface (E_{eff}) as functions of gate voltage. Electric filed intensities are supressed for Inversion-, Intrinsic- and Accumulation-Mode MOSFETs in that order at a same V_{gs}.

Fig. 4 saturation drain current (I_{dsat}) at V_{ds}=1.0 V when E_i is at 6.0 MV/cm for various Si channel doping conditions as functions of t_{SOI}. The result shows that Accumulation-Mode MOSFETs can gain the current drivability for a same t_{SOI}.

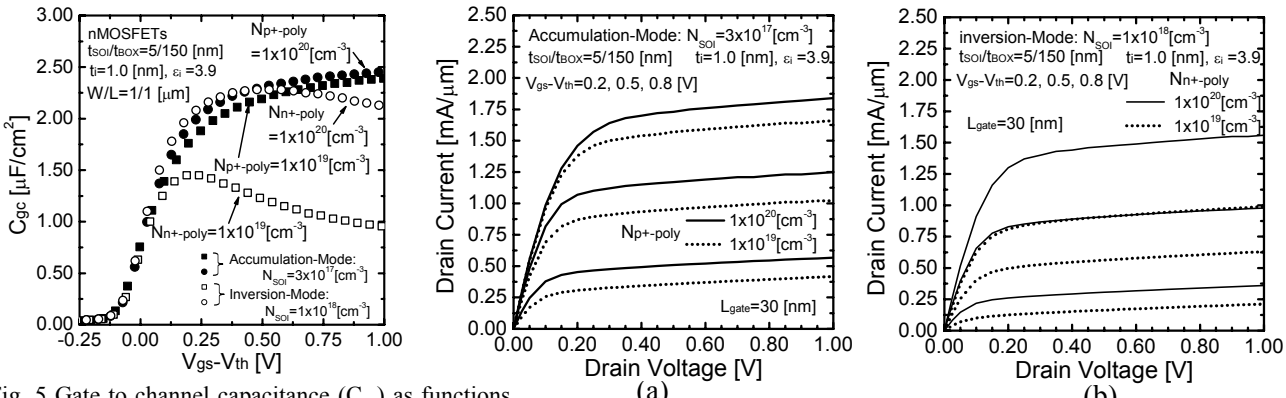

Fig. 5 Gate to channel capacitance (C_{gc}) as functions of gate overdrive voltage for Accumulation- and Inversion-Mode nMOSFETs with poly-Si gate electrode of which impurity concentration is varied from $1x10^{19}$ to $1x10^{20}$ cm^{-3}, respectively. The poly-depletion effect does not occur for the Accumulation-Mode MOSFETs.

Fig. 6 I_{ds}-V_{ds} characteristics of (a) Accumulation-Mode nMOSFETs and (b) Inversion-Mode nMOSFETs with poly-Si gate electrode of which impurity concentration is varied from $1x10^{19}$ to $1x10^{20}$ cm^{-3}, respectively. L_{gate}=30 nm. Accumulation-Mode MOSFETs maintain the high current drivability even when Np^+-poly-Si is $1x10^{19}$ cm^{-3}.