Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 414-415

P-3-5 In-situ comparison of Si/High-K and Si/SiO_2 interface properties in FD SOI MOSFETs operated at low temperature

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1. Abstract

Detailed measurements of front and back channel characteristics in advanced SOI MOSFETs are used to reveal the transport properties at the corresponding Si/High-K and Si/SiO_2 interfaces. Low-temperature operation magnifies the difference between these two interfaces in terms of carrier mobility. The mobility is lower at the Si/High-K interface and increases less rapidly at low temperature, reflecting more complex scattering mechanisms. We also discuss the short-channel effects and the difference between N and P channels.

2. Introduction

High-K dielectrics are dramatically needed for further CMOS scaling even if their properties are inferior to those of SiO_2 [1]. The comparison is nourished by separate measurements performed on High-K and SiO_2 based MOSFETs, the processing of which is more or less different. SOI MOSFETs offer the possibility of *in-situ* comparison, within the same transistor, simply by probing the front (Si/High-K) and back (Si/SiO2) channels. In this paper we combine this methodology with low-temperature measurements in advanced SOI MOSFETs.

3. Experiments

STI-isolated MOSFETs were fabricated on UNIBOND SOI wafers with a buried oxide thickness of 145 nm and an initial silicon film thickness of 70 nm. The transistor channel was left un-doped. A 25 Å thick HfSiON gate dielectric was deposited by ALCVD. The gate stack was completed by deposition of TiN (by PVD) and poly-silicon. The final silicon film thickness in the channel is approximately 10 nm. An offset spacer constituted with SiO2/Si3N4 is formed to protect the metal gate and isolate the gate stack from the upcoming elevated source/drain (SD) extensions. A double selective epitaxial is chosen to optimize the SD architecture [2], first in the LDD regions (after offset spacer formation) and then in the SD regions (after SD spacer formation). The silicon SD film thickness is 35 nm total. The tilted LDD implantation was performed prior to SD spacer formation. Finally, these structures received a 1080°C SD spike anneal for a few seconds and NiPt silicidation. The device structure is schematically illustrated in Figure 2 (inset).

Measurements were performed on both N and PMOS transistors, with short (L = 40 nm) and long (L = 1 µm) gate lengths, in the temperature range 77–300 K. Fig. 1 shows the variation of transconductance g_m versus gate voltage V_G at different temperatures T. The threshold voltage, sub-threshold slope and other parameters were extracted as in [3]. The series resistance (160 Ωµm for NMOS and 100 Ωµm for PMOS at 300 K) was calculated from the mobility attenuation factor [3].

Before discussing the mobility behaviour, we need a reliable extraction technique. The Y function method is frequently used but needs to be revisited for low temperature. The classical function, defined as $Y = I_d/(g_m)^{1/2}$, normally results in a linear variation with V_G and the slope yields the carrier mobility [4]. However, Fig.2 shows that the curves $Y(V_G)$ become strongly super-linear at low temperature leading to mobility overestimation (see also Fig.4). In order to overcome this issue, we use a corrected function $Y_n(V_G) = (I_d^2/g_m)^{1/n}$ proposed in [5]. Parameter *n* is adjusted to linearize the curves (Fig.3) before extracting the mobility [5]. Fig.3 shows the difference between the corrected function Y_4 and the classical function Y_2. Our measurements indicate that parameter *n* also varies with channel length and type.

Figure 4 compares mobility µ(T) curves obtained with different methods. Note the mobility overestimation with the classical function Y_2 and the good correlation between function Y_4 and transconductance peak. This correlation suggests a relatively small series resistance effect and shows the actual mobility behaviour at low T.

4. Mobility analysis and discussion

Typical mobility curves for the front and back channels of NMOS are reproduced in Fig. 5. Fig.6 gives a synthetic view of our systematic results. For the sake of comparison, the mobility variation with temperature is normalized with respect to room temperature values: [µ(T) - µ(T=300K)]/µ(T=300K). From Figs. 5 and 6 several trends are revealed:

(i) The front-channel mobility (Si/High-K interface) is reasonable but consistently lower than at the back channel (Si/SiO_2).

(ii) The back-channel mobility variation with temperature shows the dominant role of acoustic phonon scattering. The front-channel mobility improves less rapidly at low temperature, denoting the contribution of an additional mechanism (remote Coulomb scattering) at the Si/High-K interface. Since the mobility values are measured at low effective field, the impact of surface roughness is minor.

(iii) In shorter channels, the mobility variation with temperature is significantly attenuated. Besides a subsisting series resistance effect, we show that the presence of implantation-induced neutral defects is responsible for extra scattering [6]. These defects are located near the S/D regions and become effective in short-channels.

(iv) N and P channels exhibit similar qualitative behaviours and different quantitative trends.

The key issues briefly mentioned above will be addressed in detail. The discussion is based on the correlation of mobility variations at low temperature with the shift of other device parameters. Fig. 7 shows the subthreshold swing variation which is quasi-linear in all cases. In long channels, the swing is close to the ideal value. This implies that the density of traps at the Si/High-K and Si/$Si0_2$ interface is low and cannot be invoked to explain the mobility degradation in the front channel. No Fermi level pinning was observed. For 30-40 nm devices, the swing increases due to short-channel effects. The threshold voltage increases moderately at low temperature (< 1mV/K, Fig.8), as it could be expected for fully-depleted transistors. The short-channel effect is minimized for front-channel NMOS, reflecting a more effective optimization of the source/drain raised regions. Another interesting feature that will be described is the change in the interface coupling coefficient with temperature.

5. Conclusion

The transport properties at the Si/HfSiON interface are degraded as documented by direct comparison with the Si/SiO_2 interface. The front-channel mobility is lower than the back-channel mobility for long and short devices as well as for N and PMOSFETs. This degradation is visible in the entire temperature range. It is related to Coulomb scattering centres rather than to additional Si/HfSiON interface traps.

References
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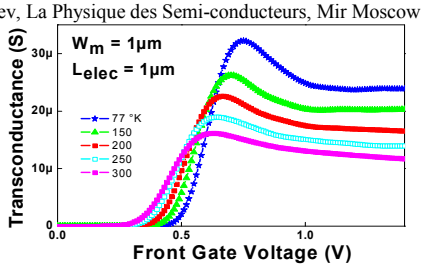

Fig.1: Transconductance versus front-gate voltage in a long n-channel SOI MOSFET for various temperatures.

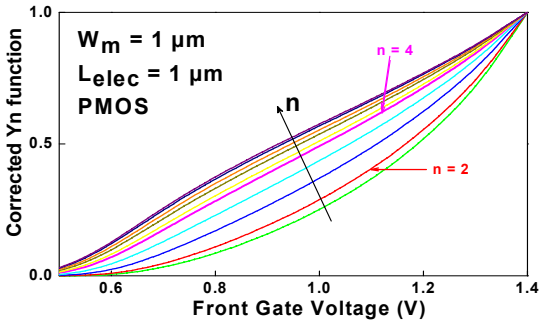

Fig. 3: Normalized variations of the corrected Y_n function versus front gate voltage. Experiment performed at 77 K.

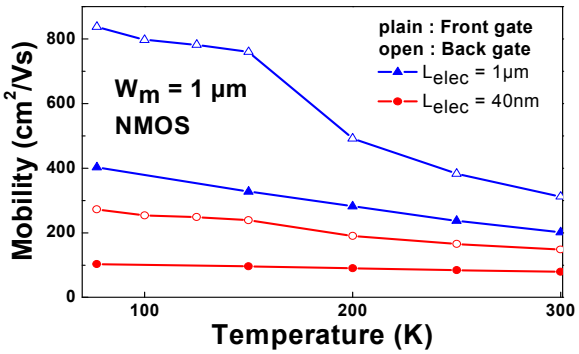

Fig.5: Comparison of mobility variation as a function of temperature for short/long and front/back channels in NMOS.

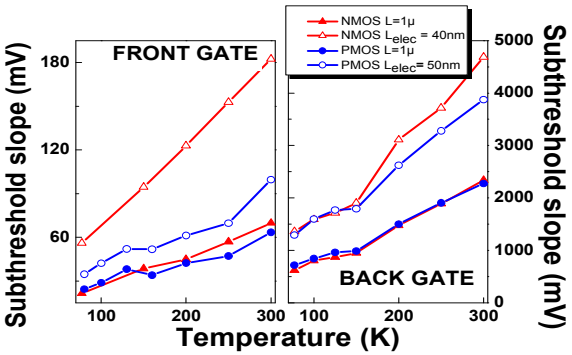

Fig.7: Subthreshold swing versus temperature for various transistors: short and long, NMOS and PMOS, front and back channels.

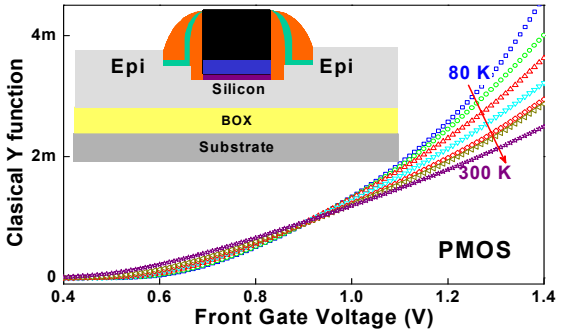

Fig.2: Variation of Y functions versus front-gate voltage in PMOSFETs operated at low temperature. The insert shows the schematic configuration of SOI transistors with double epitaxial growth in source/drain regions.

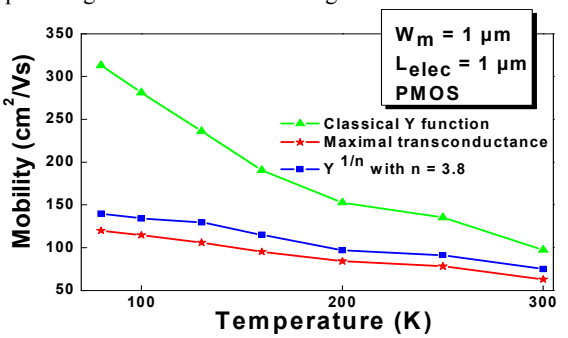

Fig.4: Comparison of mobility versus temperature curves extracted by different methods: classical function $Y = Y_2$, corrected function Y_4 and transconductance peak.

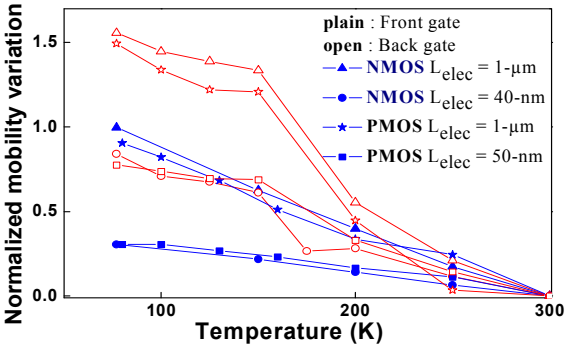

Fig.6: Normalized mobility variation with temperature, defined by [µ(T)/µ(T=300K) – 1], in various devices: short/long, NMOS/PMOS and front/back channels.

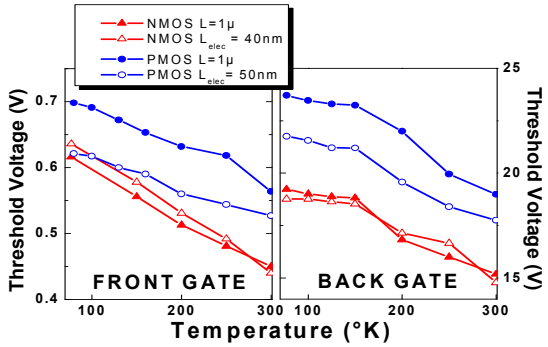

Fig.8: Threshold voltage versus temperature in various transistors: NMOS/PMOS, short/long and front/back channels.