Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 418-419

P-3-7

SiGe Recessed Source-Drain (RSD) Stressors for PMOS: Effect of Device Integration Flow and Increased Ge Content on Electrical Performance

V. Machkaoutsan[1], P. Verheyen[2], P. Tomasini[3], G. Eneman[2,4,5], R. Loo[2], P. Absil[2], S.G. Thomas[3], J.P. Lu[6], J.W. Weijtmans[7] and R. Wise[7]

[1]ASM Belgium N.V., Kapeldreef 75, 3001 Leuven, Belgium
Phone: +32 (0) 16 28 89 16; E-mail: vladimir.machkaoutsan@asm.com;
[2]IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[3]ASM America Inc., 3440 East University Drive, Phoenix, AZ, 85034, USA
[4]Catholic University of Leuven, 3000 Leuven, Belgium
[5]Fund for scientific research Flanders, Brussels, Belgium
[6]Texas Instruments assignee to IMEC, Kapeldreef 75, 3001 Leuven, Belgium
[7]Texas Instruments, 13121 TI Blvd, Dallas, TX 75243

1. Introduction

Over the last few years SiGe epitaxial layers selectively grown in Recessed Source-Drain (RSD) regions of transistors for strain engineering have been demonstrated as a key enabling technology for PMOS drive current improvements, thus relieving the pressure on further transistor scaling [1, 2].

The typical Ge content of the epilayer is ~20%. In order to further increase the channel stress level and, consequently drive current (I_{ON}), it is desirable to increase the germanium concentration in the RSD region. At higher stress levels, however, critical thickness is dramatically decreased. Therefore, the range of Ge content having practical growth rates is narrowed.

In this paper we report on the successful integration in PMOS devices of SiGe RSD stressors with increased [Ge].

2. Experimental

PMOS $Si_{1-x}Ge_x$ RSD devices were fabricated on 200mm n-type substrates: after standard Shallow Trench Isolation, and n-well implants, the gate stack was formed, consisting of 100nm poly Si on top of a 1.4 nm nitrided oxide. Gate patterning was done using an oxide hardmask (HM). This HM was conserved until after the $Si_{1-x}Ge_x$ deposition, in order to protect the gate stack during recess etch and epitaxial regrowth. After extension and halo implants, nitride spacers were formed. After spacer processing, the source-drain areas were recessed with etch depth ranging from 40 nm to 80 nm. These cavities were filled with *in-situ* B doped $Si_{1-x}Ge_x$ layers with [Ge] ranging from 20 to 40% using an Epsilon® CVD tool manufactured by ASM. The Epsilon® is a horizontal, single wafer, load-locked reactor, featuring lamp heating and rotated graphite susceptor in a cold wall quartz tube. By carefully balancing process parameters we have achieved an impressive ~70 nm/min growth rate for a fully stressed, defect free $Si_{0.8}Ge_{0.2}$ layer. For all splits, a 25 nm thick $Si_{0.8}Ge_{0.2}$ elevation was grown on top of the RSD stressors providing sacrificial material for Ni silicidation (Fig. 1).

Implantation/junction anneal schemes

To determine the effects on the SiGe epitaxy within the sequence of the process flow with respect to the Heavily Doped Drain (HDD) implantation and anneal, three epitaxy integration schemes were implemented:

i. HDD implantation and anneal done prior to RSD formation (HDD before Epi).

ii. HDD implantation and junction anneal steps implemented after SiGe epitaxy (HDD after Epi).

iii. Only junction anneal step is implemented after epitaxy (no HDD). In this case we rely solely on *in-situ* B doping of S/D.

It should be noted here that in the first and latter cases, the poly Si gate is B implanted prior to the HM deposition.

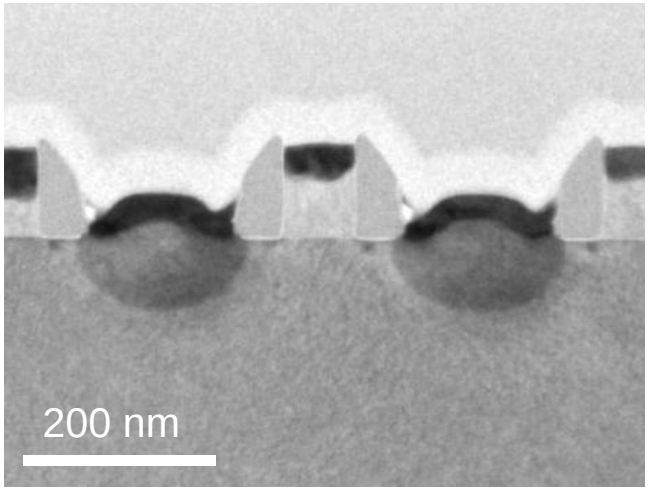

Fig. 1. A XTEM image of PMOS dense structures with the $Si_{0.7}Ge_{0.3}$ RSD stressors implemented in the 60 nm deep recess. A 25 nm thick $Si_{0.8}Ge_{0.2}$ elevation was grown on top of the RSD stressors providing sacrificial material for Ni silicidation.

3. Results and discussion

"HDD before Epi" vs. "HDD after Epi"

Device integration flows where implantation and anneal steps were done after SiGe epitaxy (HDD after Epi) yield superior electrical performance compared to the "HDD before Epi" ones. For example, one of the best I_{ON} improvements in this experiment (~40% compared to the Si reference wafer) was demonstrated by a 50 nm $Si_{0.7}Ge_{0.3}$ "HDD after Epi" split (Fig. 2). This corresponds to an I_{ON}

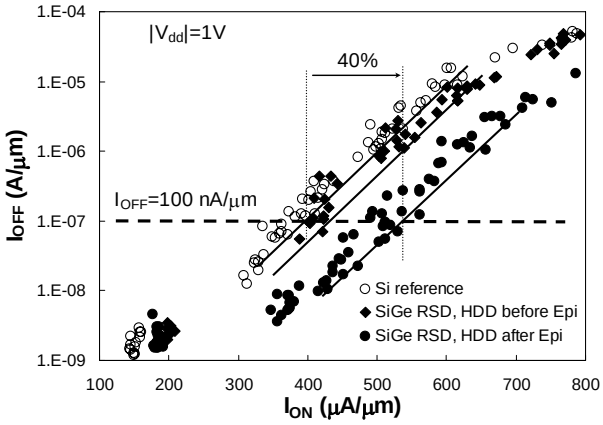

Fig. 2. The I_{ON}/I_{OFF} trade-off for 50 nm thick $Si_{0.7}Ge_{0.3}$ stressors. The "HDD after Epi" split shows 40% better I_{ON} performance compared to the Si reference devices. The "HDD before Epi" split shows only 10% I_{ON} improvement.

of 530 μA/μm at $|V_{dd}|$=1V and was demonstrated in 50-60 nm L_G devices that meet the 100 nA/μm I_{OFF} specification.

In contrast to "HDD after Epi", "HDD before Epi" splits with similar SiGe epitaxy process parameters yield considerably lower device performance. For example, a 50 nm $Si_{0.7}Ge_{0.3}$ "HDD before Epi" split shows only ~10% I_{ON} improvement (420 μA/μm at $|V_{dd}|$=1V). In addition, "HDD before Epi" splits exhibit poor V_t roll-off behavior. As a result, only devices with longer gates (~90 nm) meet the I_{OFF} specification. The average channel stress and, therefore, the I_{ON} performance are reduced.

Lower I_{ON} is correlated with higher inversion oxide thickness (T_{INV}) values for "HDD before Epi" splits. This is most probably a manifestation of boron deactivation effect induced by the epitaxy thermal budget. Deactivation leads to poly depletion at the oxide interface and, potentially, to the S/D series resistance increase. Both effects will result in a reduced I_{ON}.

"HDD after Epi" vs. "no HDD"

Fig. 3 shows the effect of post-epitaxy HDD implantation on the on-state current at $|V_{dd}|$=1V and I_{OFF}=100 nA/μm for different [Ge] and recess depth values. It can clearly be seen that in all cases the "no HDD" devices demonstrate similar or better I_{ON} characteristics compared to the "HDD after Epi" ones. Because of their superior on-state current performance, in the following section we will focus on the "no HDD" devices.

Recess depth and [Ge] effect

As can be seen in Fig. 3, both recess depth and [Ge] conditions have a strong influence on the I_{ON} characteristics. For the $Si_{0.8}Ge_{0.2}$ stressors, the on-state current shows continuous improvement with the etch depth increase. The highest I_{ON} demonstrated by the $Si_{0.8}Ge_{0.2}$ stressors is 550 μA/μm at 100nA/μm I_{OFF}. Device performance of the $Si_{0.7}Ge_{0.3}$ splits is considerably better than that of the $Si_{0.8}Ge_{0.2}$ ones, however it saturates at 570 μA/μm for the etch depth equal to 60nm or higher. Increasing [Ge] beyond 30% does not result in further I_{ON} improvement either. The best $Si_{0.6}Ge_{0.4}$ stressors (40 nm recess depth) perform just as good as the 80 nm $Si_{0.8}Ge_{0.2}$ (550 μA/μm). The abovementioned electrical results are in a very good agreement with Nomarski microscope observations revealing higher dislocation density (not shown) in the $Si_{1-x}Ge_x$ stressors of the underperforming devices. These observations can be explained by a (partial) strain relief in the SiGe stressors caused by one of the following factors or combination thereof:

i: A $Si_{1-x}Ge_x$ epilayer can (partially) relax by the formation of misfit dislocations when its thickness exceeds the critical value for a given [Ge] and a growth temperature.

ii: Junction activation anneal can result in the formation of misfit dislocations at the $Si_{1-x}Ge_x$/Si interface, leading to the (partial) strain relaxation.

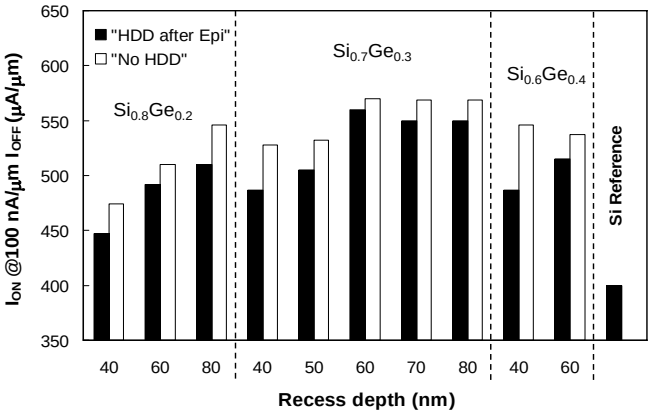

Fig. 3. Effect of the post-epitaxy HDD implantation on I_{ON} at $|V_{dd}|$=1V and I_{OFF}=100 nA/μm for different [Ge] and recess depth conditions. For all splits considered in this experiment, the "no HDD" devices show similar or better performance than the "HDD after Epi" ones.

4. Conclusions

This paper discusses the implementation of *in-situ* B doped $Si_{1-x}Ge_x$ stressors with increased [Ge] into the S/D regions of PMOS devices to boost transistor performance. It has been demonstrated that skipping the HDD implantation leads to superior device performance provided that the junction activation anneal is done after the SiGe epitaxy step. More than 40% I_{ON} improvement compared to the Si reference is demonstrated for a $Si_{0.7}Ge_{0.3}$ stressor grown into a 60 nm deep S/D recess. Increasing [Ge] and/or recess depth beyond these values does not result in further performance improvement. This effect is shown to result from a partial $Si_{1-x}Ge_x$ strain relaxation.

Acknowledgements

The authors would like to thank G. Geypen and H. Bender (IMEC) for TEM analysis.

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