Extended Abstracts of the 2007 International Conference on Solid State Devices and Materials, Tsukuba, 2007, pp. 420-421

P-3-8

Combined Effects of an Epitaxial Ge Channel and Si Substrate on Ge-on-Si MOS Capacitors and Field Effect Transistors

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1. Abstract

Electrical characteristics of MOS devices fabricated on Ge epitaxial layers grown on Si substrates exhibit a strong dependence on layer structures, such as the Ge epitaxial layer thickness, Si cap layer, and Ge channel doping. This dependence in Ge-on-Si devices is caused by different material parameters of Ge and Si.

2. Introduction

Recently, Ge pMOSFETs have been demonstrated with enhanced carrier mobility by using high-k gate dielectrics with surface passivation techniques [1-6]. However, non-ideal capacitance-voltage (C-V) characteristics, such as low frequency behavior in inversion, frequency dispersion in accumulation, hysteresis, and positive threshold voltage, have been reported on Ge channel MOS capacitors [7-8] and transistors [1-2]. Ge-on-Si heterostructures, which is a practical approach to alternative channel MOSFETs, reflect the combined effects of two semiconductors because of their different material parameters, such as bandgap energy (E_g), intrinsic carrier concentration (n_i), and permittivity (ε). In this paper, we address their impacts on MOS capacitors and MOSFETs fabricated on Ge epitaxial layers on Si substrates.

3. Device Fabrication

The process flow for Ge MOS capacitors and transistors is summarized in Fig.1. High quality epitaxial Ge layers are selectively grown on shallow trench isolation-formed n-Si (100) substrates. In gate stack, a 50Å atomic layer deposition (ALD) high-k gate dielectric is deposited with nitride passivation followed by sputtering of the TaN metal gate. Fig.2 shows a cross-sectional TEM image of the gate stack. For further processing on Ge transistors, the source/drain (S/D) junctions are ion implanted and activated at a relatively low temperature. Process variables include the Ge epitaxial layer thickness, Ge channel doping, and Si cap layer. The epi-Ge layers are fully relaxed and oriented in the (004) direction, as determined by x-ray diffraction (XRD) in Fig.3. The reciprocal space mapping shows an in-plane lattice constant of 5.647Å and out-of-plane lattice constant of 5.661Å, which results in 95% relaxation.

4. Results and Discussion

We first analyze the effect of the Ge epitaxial thickness (20, 30, and 65nm) on Ge MOS capacitors in Fig.4. Low frequency behavior in inversion is in good agreement with the results recently reported with bulk Ge MOS [8]. Stronger low frequency behavior observed at 100kHz in our epi-Ge MOS is associated with an enhanced generation rate for minority carriers due to inevitably formed structural defects in the Ge epitaxial layers as well as the intrinsic low E_g (or high n_i) of Ge. In addition, we found that low frequency behavior diminishes as the epi-Ge becomes thinner. This confirms intrinsic low frequency behavior due to Ge and the influence of the combined effects of Ge and Si on inversion capacitance of Ge-on-Si MOS capacitors. The flat-band voltages are identical regardless of Ge thicknesses. The threshold voltages (V_t), however, vary with Ge thickness, as will be shown in Ge MOSFETs. Frequency dispersion in accumulation, in Fig 5, is significantly reduced as is hysteresis (from 0.6V to less than 0.1V) after Si cap processing between the high-k and epi-Ge, which suggests improved interface state characteristics with a SiO_2 interfacial layer passivation. Low frequency behavior in inversion, however, still remains because minority carrier generation occurs in the Ge channel. Fig.6 shows a very low gate leakage current density of $<1x10^{-5}A/cm^2$ at V_g=1V with a capacitance equivalent thickness (CET) of 17Å from 50Å ALD HfO_2, which indicates a well-optimized gate stack and high-quality Ge epitaxial layers.

In fabricating Ge MOSFETs, we have compared Ge epitaxial layer thicknesses (30 to 120nm) in Fig. 7. In agreement with other Ge pMOSFETs built on bulk-Ge [1] or ~2μm thick epi-Ge [2], our thick Ge channel layers show positive V_t. According to our theoretical calculation, the V_t of the Ge pMOSFETs shifts toward positive relative to the Si pMOSFETs. The V_t, which is proportional to $-Q_d/C_{ox}$, shifts more toward negative as the undoped epi-Ge channel becomes thinner. This shift is due to an increase in a positive depletion charge (Q_d) of the n-Si substrate or an increase in the Si portion of the depletion region. A negative V_t has been achieved with our thin 30nm epi-Ge channels for the first time..

The subthreshold swings in Fig.8 increase as the Ge layers become thicker, which is associated with an increase in junction capacitance and leakage current as shown in Fig.9 due to the higher ε of Ge (16) than Si (11.9). For a thick epi-Ge channel, S/D-junctions are confined in a sufficiently thick epi-Ge layer in which band-to-band tunneling (BTBT) current is high because of high ε and low E_g. For a thin epi-Ge channel, the S/D junctions are formed across the epi-Ge layer and Si substrate, which reduces the junction area in the epi-Ge and increase the junction area in Si. Therefore, the BTBT current is suppressed. The C-V measured from the Ge pMOSFET exhibit an EOT of ~17Å. Fig.10 shows the drain current-gate voltage (I_d-V_d) curves for a further optimized Ge pMOSFET with a 2nm-Si cap layer. Fig.11 compares the normalized transconductance (Gm) of the epi-Ge channel (EOT=~17Å) over the optimized Si channel (EOT=14Å with high-k/metal

gate). A mobility enhancement of 2x (high field) ~ 3x (low field) over the Si channel has been readily achieved.

5. Conclusions

We studied the effect of Ge-Si heterostructures on the characteristics of Ge MOS capacitors and transistors. The thickness of the Ge epitaxial layer, Ge channel doping, and Si cap layer determines the electrical parameters of Ge-on-Si MOS devices. Therefore, understanding their combined material properties, such as intrinsic carrier concentration, permittivity, and bandgap energy is important to implementing future high performance Ge-on-Si MOSFETs.

References

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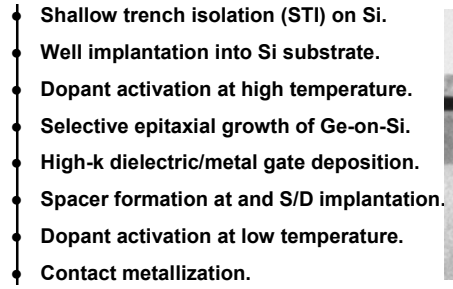

Fig.1 Process flow of Ge MOS capacitors and transistors on the Ge epitaxial layers selectively grown on Si (100) substrates.

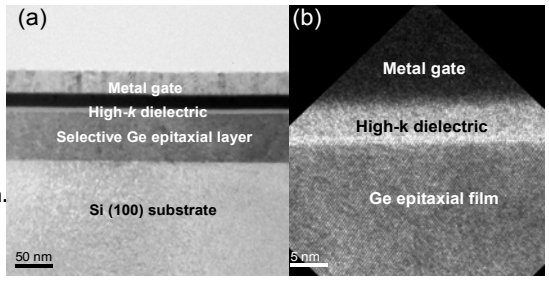

Fig.2 Bright-field and (b) high-resolution XTEM images of Ge MOS capacitors with 50Å high-k gate dielectric/metal gates on high-quality 65nm Ge epitaxial layers selectively grown on Si (100) substrates.

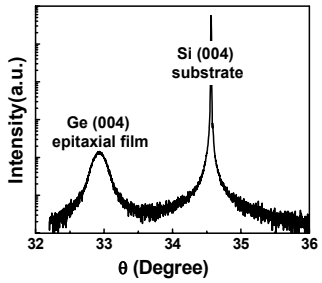

Fig. 3 XRD of Ge-on-Si with two peaks due to the Bragg reflection from epi-Ge (004) and Si (004) planes.

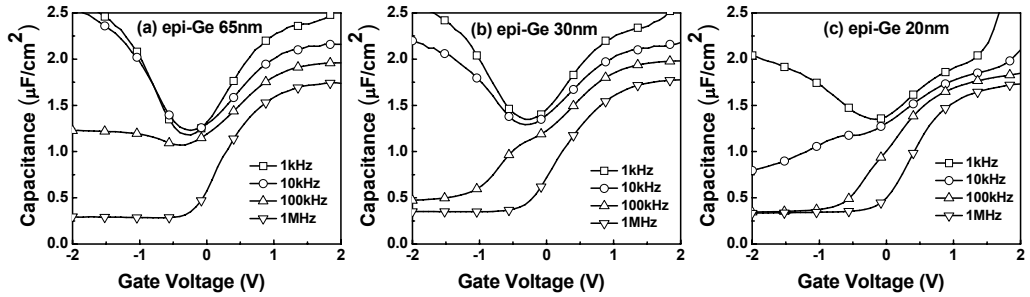

Fig. 4 Effect of the Ge epitaxial layer thickness of (a) 65, (b) 30, and (c) 20 nm on Ge MOS capacitors at room temperature. Low frequency behavior in inversion, which is attributed mostly to low bandgap energy (or high n_i) of Ge and partially to the defects in the Ge epitaxial layers, is more evident on thick Ge-on-Si MOS capacitors.

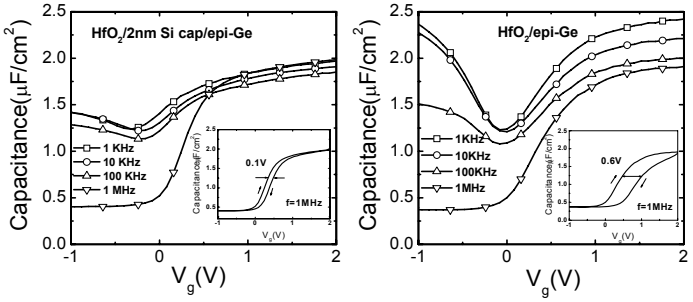

Fig. 5 Reduction in hysteresis and frequency dispersion in accumulation of Ge-on-Si MOS capacitors (a) with, and (b) without a 2nm-Si cap layer between high-k and epi-Ge. Low frequency behavior in inversion, however, still remains because minority carrier generation occurs in the Ge-on-Si channel.

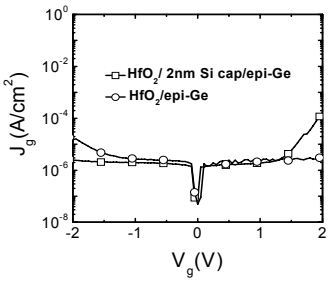

Fig. 6 Very low gate leakage current density of Ge MOS capacitors with or without Si cap layer between high-k and epi-Ge.

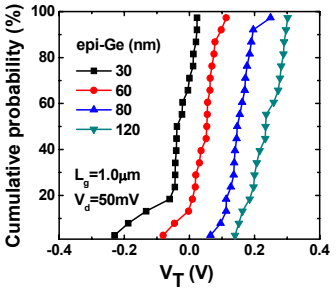

Fig. 7 Variation in threshold voltages of Ge-on-Si pMOSFETs as a function of the Ge epitaxial layer thickness grown on Si substrates.

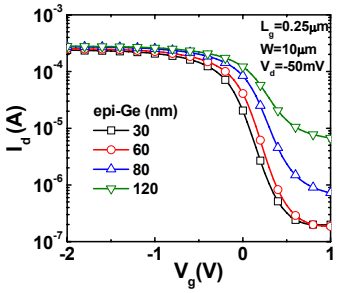

Fig. 8 Subthreshold swings of Ge-on-Si pMOSFETs increase as the Ge become thicker because of junction capacitance and leakage current effect.

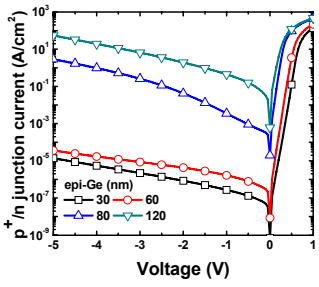

Fig. 9 Thin Ge shows lower leakage current than thick Ge because the junctions are formed in Si, which reduces BTBT leakage current.

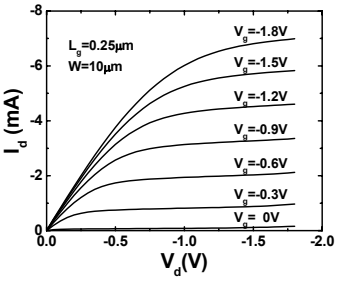

Fig. 10 Well-behaved Id-Vd curves for a further optimized Ge pMOSFETs with gate length of 0.25μm fabricated on 65nm thick Ge epitaxial layers.

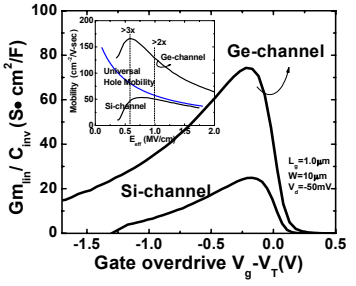

Fig. 11 Hole mobility enhancement of a Ge pMOSFET with >3x at peak mobility and >2x at 1MV/cm over the optimized high-k Si channel.