Investigation of Impact Ionization in Strained-Si nMOSFETs

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1. Introduction

Tensile strained-Si nMOSFETs have been much attractive for high-speed and low-power logic CMOS technology because of its electron mobility enhancement [1]. Typically, the biaxial tensile strain is to study a thin epitaxial Si grown on a relaxed Si_{1-x}Ge_x structure. Once the hetero-structure is formed, the strain-enhanced electron mobility can be attributed to a lower conductivity effective mass in the occupied Δ_2 valleys and the suppression of inter-valley scattering between the Δ_2 and Δ_4 valleys [2]. On the other hand, another reliability issue is that the band-gap narrowing due to strain in Si enhances the impact ionization (II) rate [3], which generates more hot electrons. Although the strain-induced the enhancement of II rate has previously been presented [4], the physical origin is still a matter of debate. This is due to greatly increasing the II in the presence of the severe self-heating effect [5]. In addition, the opposite result for the II rate has also been reported by Nicholas et al [6].

The aim of this paper is to utilize the tensile strained-Si grown on a relaxed $Si_{1-x}Ge_x$ structure with varying Ge contents and strained Si cap layers to clarify the II characteristics in strained Si nMOSFETs.

2. Experimental

Detailed process of strained Si nMOSFETs with a gate dimension of W/L=10µm/10µm had been published elsewhere [7]. The unstrained Si device, here called as a control sample, was fabricated by using a conventional CMOS process for comparison. The strained Si/Si_{1-x}Ge_x structure and experimental setup of II are schematically illustrated in Fig. 1. The Ge contents, x, with 15% and 20% could be quantified by XRD analysis. Furthermore, the strained-Si cap layer with two thicknesses of 10nm and 15nm was grown on each Si_{1-x}Ge_x substrate. The final Si cap layer consumed by surface clean and gate oxidation process was determined to be around 3nm and 8nm, respectively, via the cross-section of TEM [8]. The thinner Si cap thickness below 5nm has to consider the Ge out-diffusion factor affecting the scattering in strained Si/SiO₂ interface [9]. The device with a relatively long channel of 10 µm can neglect the series resistance of source and drain, and the self-heating effect as previously reported in [6]. The electron mobility was extracted from a well-known split C-V technique.

3. Results and Discussion

Figure 2 shows the comparison of electron mobility extracted from unstrained Si and strained Si nMOSFETs. Despite Ge contents changed from 15% to 20%, the

thinner Si cap thickness of 10nm including the process consumption shows no significant enhancement of electron mobility due to more scattering caused by Ge out-diffusion effect. The finding also responds to the substrate current (I_B) as shown in Fig. 3, implying that the higher mobility can produce more energetic electrons by a lateral acceleration and then lead to the increase in I_B via the II. Another feature of the tensile strained-Si is the band-gap narrowing due to strain in Si. Figure 4 clearly indicates that the voltage difference between $I_{\rm G}$ and $I_{\rm B}$ in strained Si is smaller than that in unstrained Si, showing a smaller band-gap value and also matching the E_G=1.11-0.6x [10]. In order to further clarify the II characteristics, we employ the strained Si nMOSFETs with varying Ge contents and strained Si cap layers to evaluate the II multiplication coefficient of M-1 ($=I_B/I_S$), defined as the ratio of I_B to I_S . Under the same gate overdrive of 0.6V, various I_s and I_B by the II measurement are shown in Fig. 5, indicating the simultaneous increase in I_B with increasing Is via the II. Further, no significant difference in M-1 between unstrained Si and strained Si is found in Fig. 6. However, even though a smaller band-gap value and more scattering caused by Ge out-diffusion, the M-1 in strained Si is quite consistent with that of unstrained Si. Moreover, under a high V_{DS} region the I_B measured with source floating shows a negligible diode (drain-tosubstrate) leakage current compared to I_B measured with source grounded, as shown in Fig. 7. The origin of I_B enhancement is attributed to the increase in I_S with a lower effective mass. That is, the electrons prefer to populate the lowered Δ_2 valleys, implying the reduction in the number of available free-energy states for Δ_2 valleys. It means that the II characteristics in strained Si don't experience the band-gap narrowing and look like those in unstrained Si. Therefore, this can be strongly associated with reduced the number of density of states [6] and further applied to the explanation of the improved hot-electron reliability [11].

4. Conclusions

The II in strained Si nMOSFETs with varying Ge contents and strained Si cap layers has been experimentally investigated. The origin of the I_B enhancement in strained Si is attributed to the increase in I_S with a lower effective mass in Δ_2 valleys. Even though the band-gap narrowing and more interface scattering, no significant difference in M-1 between unstrained Si and strained Si is found. This implies that the II characteristics in strained Si are similar to those in unstrained Si without the band-gap narrowing effect and in support of the argument of the reduced density of states proposed by Nicholas et al.

References

[1] J. Welser et al., IEDM, 1994, p. 373.

[2] T. Vogelsang et al., IEEE Trans. Electron Devices (1992) 2641.

[3] M. F. Lu et al., IRPS, 2004, p. 18.

[4] N. S. Waldron et al., IEEE Trans. Electron. Devices (2005) 1627.

[5] K. A. Jenkins and K. Rim, IEEE Electron Device Lett. (2002) 360.

[6] G. Nicholas et al., J. Appl. Phys. (2005) 104502.

[7] Y. P. Wang et al., Jpn. J. Appl. Phys. (2005) 1248.

[8] Y. P. Wang et al., Jpn. J. Appl. Phys. (2005) 1560.

[9] G. K. Dalapati et al., IEEE Trans. Electron. Devices (2006) 1142.

[10] L. Yang et al., Semicond. Sci. Technol. (2004) 1174.

[11] D. Onsongo et al., IEEE Trans. Electron. Devices (2004) 2193.



Figure 2 Typical effective field dependence of effective mobility of unstrained Si and strained Si nMOSFETs.



Figure 4 Gate and substrate currents versus gate voltage in unstrained Si and strained Si nMOSFETs by carrier separation measurement with other terminals grounded.



Figure 6 Impact ionization multiplication coefficient $(M-1=I_B/I_S)$ as a function of drain voltage corresponding to Fig. 5.



Figure 1 Schematic illustration of cross section and experimental setup of strained Si nMOSFETs for impact ionization (II) measurement.



Figure 3 Gate overdrive (V_G - V_T) dependence of substrate current for unstrained Si and strained Si nMOSFETs under a fixed V_{DS} =2.6V.



Figure 5 Comparison of source and substrate currents in both unstrained Si and strained Si nMOSFETs under a fixed gate overdrive (V_G-V_T) of 0.6V.



Figure 7 Comparison of source and substrate currents in strained Si nMOSFETs with source grounded and floating under a fixed gate overdrive (V_G-V_T) of 0.6V.