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Electronic characteristics of charge trapping memory using Al_2O_3 dielectric

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1. Introduction

The SONOS structure has become an appealing alternative for the next-generation flash memory applications because of its numerous advantages such as film scalability, process simplicity, and power economy. However, as the nitride thickness and the gate size are reduced in nano - scale, charges are trapped close to the gate electrode and most of them are lost through the gate electrode, resulting in data loss. In order to improve the scaling properties of the devices for the sub 100nm flash technology node, high-κ materials such as Al_2O_3 are interesting alternatives to the standard dielectrics such as silicon dioxide and silicon nitride. Al_2O_3 has a large energy band gap value of 8.9eV, a large conduction band offset of 2.8eV with respect to silicon, and a dielectric constant value of 9, making it an attractive candidate as a blocking oxide. Furthermore, this structure can be achieved longer data retention and realized lower voltage programming than the conventional ONO structure. In this study, we compare SiO_2 with Al_2O_3 as a blocking dielectric in a metal-insulators-semiconductor (MONOS, MANOS) type capacitors similar to the well known SONOS and SANOS devices [1].

2. Experiments

Four samples of ONO, ONA, Si_3N_4 and SiO_2 on n-type Si substrates were prepared as shown in Table 1. The tunneling oxide was grown by thermal oxidation while the blocking oxide and the nitride layer were deposited by low pressure chemical vapor deposition (LPCVD). Rapid thermal annealing is performed in N_2 gas at 900 ℃ for 1 min.

Table 1. Thickness of the structures

	Tunneling layer(Å)	Trapping layer(Å)	Blocking layer(Å)
ONO	20	60	65
ONA	20	60	150
Si_3N_4	0	150	0
SiO_2	150	0	0

Then, either metal-oxide-semiconductor (MOS) or MIS type capacitors was fabricated for capacitance-voltage (C-V) and deep level transient spectroscopy (DLTS) measurements. Al gates with a diameter of 0.3mm were formed on the blocking layer by thermal evaporator while In contact was made on the substrate for Ohmic contacts.

3. Results

In order to investigate memory effect, C-V measurement was performed, respectively [2].

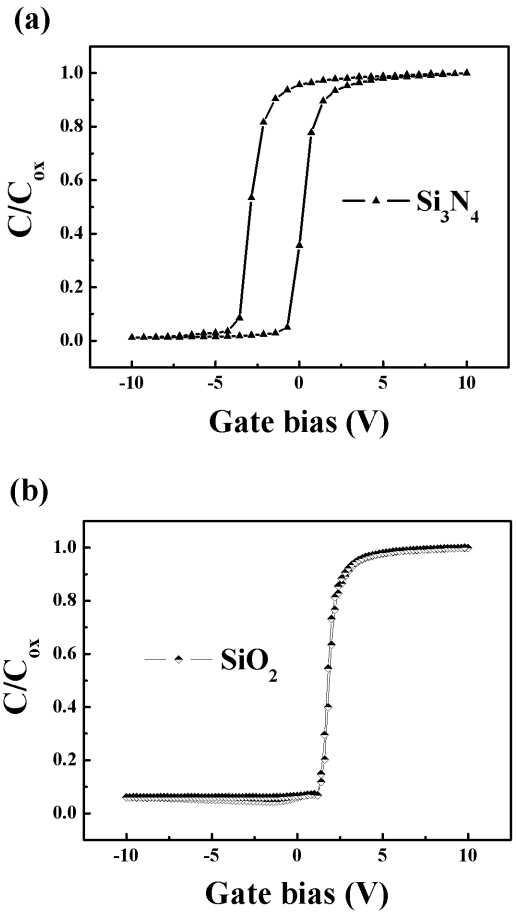

Fig. 1 CV hysteresis (a) Si_3N_4 (b) SiO_2 on n-type Si substrate

Figure 1 exhibits C-V hysteresis after bi-directional voltage sweeping. The voltage was swept between 10 and -10V. The erasing and programming voltages were fixed at -10V and 10V, respectively. The difference between the charging and discharging point, which is referred to as the "memory window", was ~3.0V for the Si_3N_4/Si (MIS) capacitor, and 0V for the SiO_2/Si (MOS) capacitor. The memory effect was not observed for the oxide layer fabricated on n-type Si substrates. Figure 2 shows C-V hysteresis curves for the ONO and ONA structures.

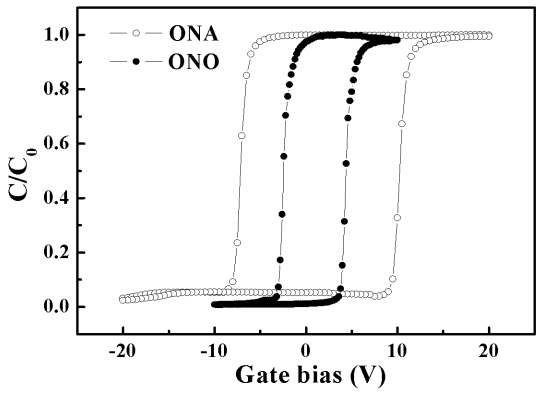

Fig. 2 CV hysteresis of ONO and ONA on n-type Si substrate

We found that leakage current was produced in the ONO and ONA capacitor at more than 10V and 20V bias sweeping condition. This bias condition is referred to as the "critical bias point". At critical bias point, structure has the maximum memory window. The maximum memory window were ~5.5V for the ONO capacitor and ~18V for the ONA capacitor

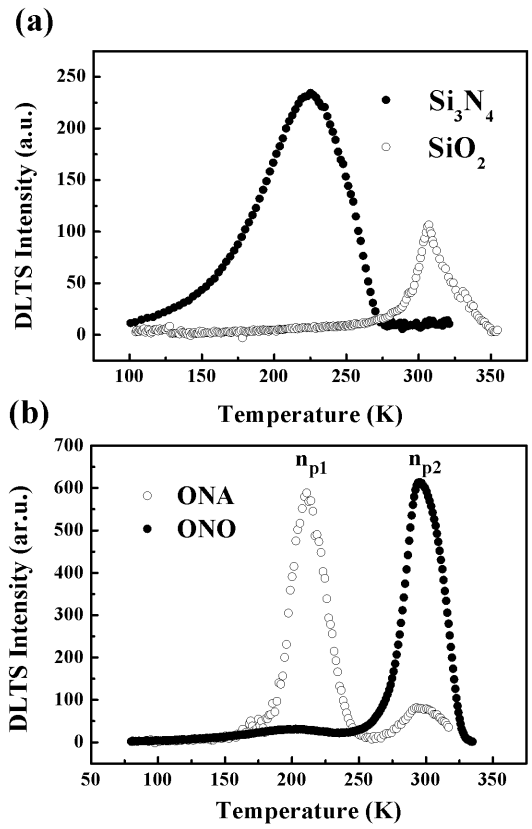

Fig. 3 DLTS signal of (a) Si_3N_4, SiO_2 (b) ONO and ONA on n-type Si substrate

The DLTS study was then performed to get more detailed information on the spatial distribution of the memory traps available in the ONO and ONA structure. Figure 3 shows the DLTS spectra measured from the Si_3N_4 (MIS), SiO_2 (MOS), ONO and ONA capacitors fabricated on the n-type Si substrates. The MIS and MOS structures were prepared as the reference for identifying the origin of the trap present in the ONO and ONA structure. In both ONO and ONA capacitor, two DLTS peaks were observed at around 200K (n_{p1}) and 300K (n_{p2}), respectively. We attributed n_{p1} and n_{p2} to the nitride traps (traps related to the nitride layer) and interfacial traps (traps related to the interface between Si and SiO_2), respectively, by comparison with the DLTS signals of the MIS and MOS capacitor.

For the ONO and ONA structures, they showed a reverse relation in its peak intensity. That is, n_{p2} representing the interface trap density was dominantly observed in the ONO structure while n_{p1} representing the nitride trap density was dominant in the ONA structure. Since the interface traps between Si and SiO_2 could be a factor that can degrade device reliability (or retention), they should be reduced This is also accounted for why the memory window of ONO is always observed to be narrower than that of the ONA structure. In this work, we carefully conclude that the ONA structure holds benefits inherently for the application to charge-trap memory device over the ONO structure. The trap activation energy (E_a) and trap concentration (N_T) of the ONO and ONA structures are listed in Table 2.

Table 2. E_a and N_T of the ONO and ONA structure

	ONO		ONA	
	E_a (eV)	N_T (cm^{-3})	E_a (eV)	N_T (cm^{-3})
n_{p1}	0.27	$2.45x10^{13}$	0.27	$2.00x10^{14}$
n_{p2}	0.54	$3.93x10^{14}$	0.55	$4.00x10^{13}$

More details on the experiment will be presented at the conference

4. Conclusions

The C-V and DLTS analyses were made for both ONO and ONA capacitors to have information on the memory effect and the origin of charge traps. The memory window and the DLTS signals related to the nitride traps were always dominantly observed for the ONA structure, compared with those of the ONO structure. Reduction in the memory window observed by C-V for the ONO structure is thought to be due to the interface traps dominant between Si and SiO_2. These results directly show that the ONA structure is more suitable than ONO for the application to charge-trap memory devices.

Acknowledgements

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References

[1] M.Specht, H.Reisinger, M.Stadele et al, *IEEE 33rd conference on. ESSDERC* (2003) 155

[2] J. S. Oh, C. J. Park, and H. Y. Cho, *ECS Trans.*, **1**, 5(2006)