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Si Quantum Dot TFT Nonvolatile Memory for System-On-Panel Applications

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1. Introduction

Poly-Si thin-film transistor (TFT) technology is the most promising candidate for the ultimate goal of building entire system on top of panel [1]. They are commonly used in liquid-crystal displays as pixel switches, drivers and peripheral control circuits [2]. The ability to include the functionality of memory will thus result in integration of different functional devices to achieve system-on-glass. Quantum dot nonvolatile memory possesses great potential for achieving this goal due to its superior retention, excellent endurance, high program/erase (P/E) speed, and low programming voltage [3]. For practical applications, room temperature operation and large threshold voltage shift per electron are required, which is made possible by small dot size and high dot density.

In this paper, we used Si quantum dot grown on Si_3N_4 as the storage layer for the poly-Si TFT memory. Si_3N_4 provides a good medium for quantum dot growth due to its rougher surface, which increases reactive sites, and thus the probability of surface reaction [4]. This means that the surface of Si_3N_4 is suitable for more uniform quantum dots with high density and small dimension. To take advantage of the nitride film characteristics while keeping high interface quality between the tunneling dielectrics and the Si substrate, oxide-nitride tunneling dielectrics is used. Using low thermal budget (<600^{o}C) for all processes, the proposed nonvolatile memory fabrication is compatible with conventional TFT processing.

2. Device Fabrication

Fig. 1 shows the schematic cross section of the device. Amorphous silicon (a-Si) layer of 100 nm was deposited by low-pressure chemical vapor deposition (LPCVD) at 550^{o}C on oxidized silicon wafers. Next, the oxide layer and nitride layer were both deposited by PECVD. The Si quantum dots were fabricated by LPCVD at 580^{o}C, 130 mTorr, for 15 sec. A high dot density of ~10^{11} cm^{-2} was obtained on the nitride surface, as shown in the SEM images of Fig. 2 (a). The Si quantum dots fabricated were about 8 nm in diameter. A 33-nm blocking oxide was then deposited by PECVD with subsequent poly-Si deposition and gate-stack patterning. The source/drain was implanted with 3x10^{15} cm^{-2} of arsenic, followed by the formation of nitride spacer. Nickel was deposited by PVD and annealed at 450^{o}C for 30 sec in N_2 ambient. After nickel removal, the wafers were heat-treated at 550^{o}C in N_2 ambient for 4 hrs to laterally crystallize the channel. The implanted dopants were simultaneously activated during this step.

3. Results and Discussion

Fig. 2 (b) shows the cross sectional TEM image of the fabricated memory. Figs. 3 & 4 show the I_d-V_g characteristics for the TFT memory. The program/erase times are 1 sec. A relatively large memory window of about 3 V can be achieved with V_g = 10 V, V_d = 8 V program operation. Program and erase characteristics as a function of pulse width for different operation conditions are shown in Fig. 5. With V_g = 10 V, V_d = 8 V, high speed (10 ms) programming performance can be achieved with a memory window of about 2.2 V. Again, excellent erase speed of about 10 ms at V_g = -9 V, V_d = 8 V for a -2.2 V shift. More importantly, over-erasure is kept to a minimum at these operating conditions. The reason is likely due to the fact that the vertical electric field decreases with decreasing amount of trapped electrons in the quantum dots by coulomb blockade effect during erasing [5]. Fig. 6 illustrates the retention capability of the TFT Si quantum dot memory device at room temperature. The threshold voltage remains unchanged up to 10^4 sec for low program operation (V_g = 8 V, V_d = 6 V). At high program operation (V_g = 10 V, V_d = 8 V), a 15% charge loss is expected for 10-year operation. The endurance characteristics are shown in Fig. 7. Despite the occurrence of significant memory window narrowing, a memory window of at least 0.8 V is sustained up to 10^5 P/E cycles. The origin of the memory window narrowing is likely due to a mismatch of distribution for injected electrons and holes. It has been shown that holes are not able to fully compensate the electrons stored during programming and erasing [6]. The uncompensated electrons will then cause the V_{th} to increase gradually over the P/E cycling. Another reason is due to stress-induced electron traps generated in the tunnel oxide during cycling. Therefore, for improved performance, a better quality of tunnel oxide is recommended. Fig. 8 shows the feasibility of the device for 2-bit memory operation. It is clear that one could employ forward and reverse reads [7] to detect the information stored in the programmed bit 1 and bit 2, respectively. During read operation, the depletion region extends over the locally trapped charge, and the programmed cell will have a higher conduction current. This is possible because the quantum dots are well separated, preventing conducting paths between adjacent nodes, minimizing lateral or vertical charge migration.

A comparison of the TFT quantum dot memory device with conventional TFT transistors fabricated by solid phase crystallization (SPC) and metal induced lateral crystallization (MILC) is presented in Table I [8]. The device V_{th} is about 1-2 V higher than that of a conventional MILC TFT transistor. This is because of the thicker gate stack used in the memory device. For the subthreshold swing (S value), and I_{on}/I_{off} ratio, the fabricated device is comparable to that of a TFT transistor.

4. Conclusion

In this work, we have successfully demonstrated the feasibility of fabricating poly-Si TFT Si quantum dot nonvolatile memory with excellent characteristics in terms of

good memory window, long retention time, high P/E speed, and good endurance. We have also shown that the device is able to function as a 2-bit memory cell and compared its performance with conventional TFT transistors. The TFT Si quantum dot memory can be ascribed as a suitable starting point for future TFT memory applications.

References

[1] A. Kumar et al. *IEDM Tech. Dig.*, pp. 515–518, 1997. [2] C. R. Kagan et al. *Thin-film transistors*, Part I, Marcel Dekker, Inc, 2003. [3] J. D. Blauwe et al. *IEEE Transactions on Nanotechnology*, pp. 72-77, 2002. [4] I. Kim et al. *IEDM Tech. Dig.*, pp. 111–114,1998. [5] Y. Lin et al. *IEEE Electron Device Letters*, pp. 154-156, 2005. [6] L. Sun et al, *Japanese Journal of Applied Physics*, pp. 3179-3184, 2006. [7] Y. Chang, et al. *IEEE Electron Device Letters*, pp. 95-97, 2004. [8] Y. Kuo. *Thin Film Transistors: Material and Processes*, *Vol. 2: Polycrystalline Silicon Thin Film transistor*. Kluwer Academic Publisher, 2004.

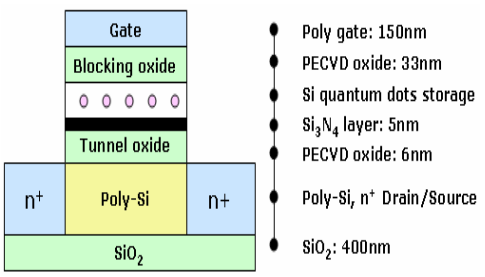

Fig. 1. Schematic cross section of TFT Si quantum dot nonvolatile memory device.

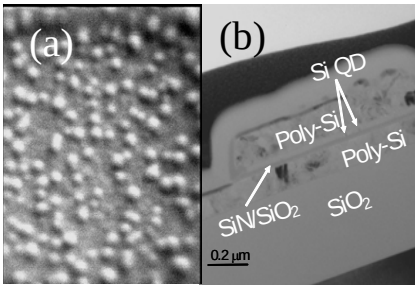

Fig. 2. (a) SEM image of Si quantum dots grown on nitride layer; (b)TEM image of cross-section

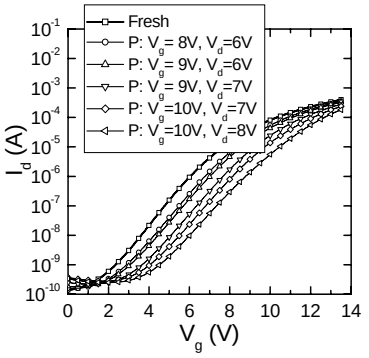

Fig. 3 I_d-V_g curves of TFT quantum dot memory at different programming voltages.

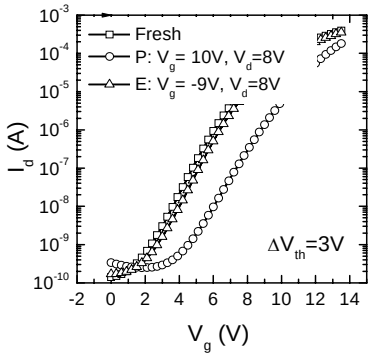

Fig. 4 I_d-V_g curves of TFT quantum dot memory at Program/Erase operation.

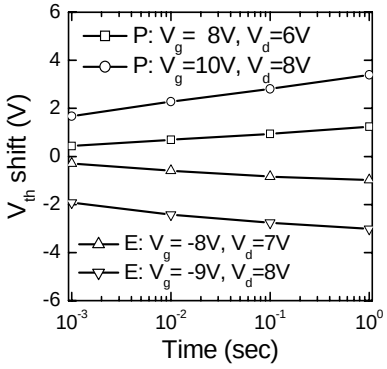

Fig. 5. Program and erase characteristics of TFT quantum dot memory. The erasing time is about 10ms.

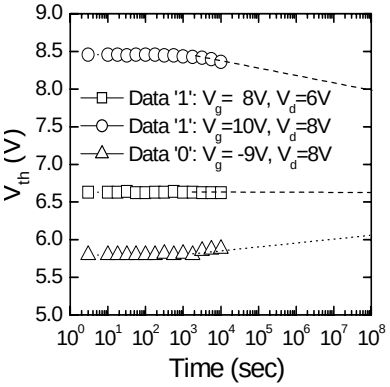

Fig. 6. Retention characteristics of TFT quantum dot memory. Low charge loss is seen after 10^4 seconds.

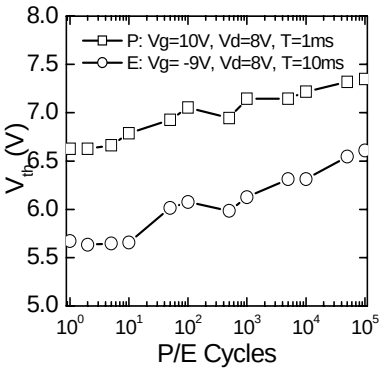

Fig. 7 Endurance characteristics of TFT quantum dot memory. Memory window narrow to about 0.8V after 10^5 P/E cycles.

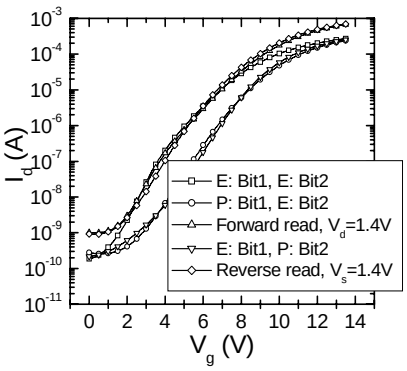

Fig. 8 2-bit memory operation. Bit 1: drain side; Bit 2: source side.

Table I Device comparison with conventional TFT transistors

Parameters	TFT transistor [8]			This work
	SPC	MIUC*	MILC	MILC
V_{th} (V)	4	3.0	3.8	5.8
S (V/dec)	-	1.1	1.4	1.2
I_{on}/I_{off}	1×10^{10}	1.4×10^{7}	9.3×10^{5}	1×10^{7}

* MIUC: Metal Induced Uni-lateral Crystallization