Delay-Correction Flip-Flops for Timing-Error Tolerant Circuit Design

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1. Introduction
As the clock frequency and circuit integrity have been increased exponentially, power consumption has also increased drastically and process variations have been becoming a big issue. One of the most effective methods for low power computation is dynamic voltage scaling (DVS) with in-situ timing-error detection. Furthermore, it is robust to parameter variations in the extremely scaled technology generations and can minimize timing and voltage margins, because supply voltage is dynamically tuned during circuit operation, or after every fabrication process is finished.

However, conventional methods for in-situ timing-error monitoring have some disadvantages: the decrease of the degree of freedom for designing circuits and the necessity of the complex recovery mechanism for timing errors.

The delay-compensation flip-flop (DCFF) automatically regulates its control signal as it finds the boundary between two successive data with error detection. The purpose of this paper is to present how DCFF can substantially solve the problems mentioned above, compared to conventional methods described in the section 2.

2. Error-Detection in Conventional Methods
Razor [1] and Canary flip-flop [2] are typical DVS systems with in-situ timing-error monitoring (Fig. 1).

Razor has a duplicated flip-flop called shadow-latch controlled by the delayed clock. Even if the timing error occurs on the main flip-flop, valid data is kept in the shadow-latch. Then, the difference between the data kept in main flip-flop and shadow-latch is detected as the occurrence of timing error and valid data are written back to the main flip-flops from shadow-latches. However, the complex circuit implementation is required because the processor has to be stalled when the timing error occurs. Moreover, the min-delay path has to be long enough to satisfy the hold-time of the shadow-latches not to destroy the data in shadow-latches by the subsequent data.

The Canary flip-flop also has a duplicated flip-flop and a delay-buffer inserted in front of it. When the timing error is about to occur on the main flip-flop, it actually occurs on the duplicated flip-flop because of the inserted delay. The difference between data of main and duplicated flip-flops is detected as the prediction of timing errors. Since valid data are kept in the main flip-flops, complex recovery mechanisms are not required. However, the max-delay constraint gets more severe because of the delay-buffers. It may deteriorate the processor performance, because max-delay path is strongly related with clock frequency, yield, and so forth.

3. Delay-Correction Flip-Flops (DCFF)
DCFF uses timing of signal transients. Timing errors are detected when the clock and data signals swing simultaneously. DCFF can detect both timing violations of max-delay and min-delay paths, although conventional methods detect only that of the max-delay. It is more advantageous as the parameter variations of transistors become more severe.

The signal name Gate is used to directly control the DCFF instead of the clock. When the slightly delayed input signal arrives to the DCFF, timing errors are detected and the Gate waits for the input signal to become stable as shown in Fig. 2. Although the delay of the input signal spreads to subsequent stages, it can be compensated by the timing margin of the next logical stage, because it is infrequent that timing-critical stages are continuous in the processor or the timing-critical path is actually activated [3].

The timings of the setup time and hold time dynamically change as the timing of the Gate signal is tuned. As shown in Fig. 3, because not only the max-delay but also min-delay paths become slow when the operation of the logical stage becomes slow, the min-delay path can be designed shorter. Therefore, DCFF keeps the degree of freedom for timing-design higher, compared to conventional methods, whose setup and hold time are fixed during the circuit design.

Fig. 4 shows the circuit implementation of the rising-edge detector. When the input signal swings from low to high, the voltage of Edge node become low sharply and go back higher level because of the inverter’s delay. This
Fig. 3  When the computational speed of logical stage changes, rising-edge timing dynamically adjust to arrival timings of data. pulse indicates timing of the rising-edges of the signal. DCFF checks the overlaps of these Edge pulses to detect timing errors. Fig. 5 shows circuit implementation of the DCFF. If the input data signal \( D \) is not stable at the moment of the rising-edge of the clock, the timing error on max-delay path is detected and the Gate keeps low till the \( D \) becomes stable. If the \( D \) swings immediately after the Gate rises, the violation of the min-delay constraint nearly occurs and it is predicted.

4. Simulation Results

Fig. 6 demonstrates the HSPICE simulation results of the DCFF behavior. It indicates how signal timing changes when the supply voltage of the previous logical stage scales and operation speed of the pervious logical stage slows down. The setup time and hold time dynamically adjust as the timing of the input signal changes. This result also indicates that DCFF works in larger voltage ranges than Canary flip-flops. The previous logical stage is 16bit Kogge-Stone adder and the clock frequency is 1GHz. This simulation is based upon the Rohm 0.18\( \mu \)m process simulation models and the normal supply voltage is 1.8 V. In another simulation, confirmed that timing errors of the min-delay path could be predicted in cases where \( D \) becomes unstable up to approximately 0.15ns after the Gate rises.

5. Conclusion

DCFF is proposed to improve the problems with the conventional in-situ timing-error monitoring methods. It can detect both timing errors of the max-delay and min-delay paths and can minimize the timing margin during circuit design. Moreover, it does not require complex recovery mechanisms like the Razor and it has been confirmed that it works in a wider voltage range than the Canary flip-flop.

Future directions of this study include evaluating how DCFF works to achieve the robust and low-power circuit design with DVS by using a whole processor prototyping. The prototype chip is being prepared now for the actual measurement.

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References