

P-5-12L

Chip-to-Chip Power Delivery by Inductive Coupling with Ripple Canceling Scheme

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1. Introduction

System in a package (SiP) is a prospecting way to reduce cost and package size of LSI [1]. Fig.1 illustrates a conceptual scheme of SiP with wireless data link and power delivery. With out bonding wire, several daughter chips such as MCU, memories stacked up on mother chip can be upgraded even after fabrication, which makes the system reconfigurable after manufacture [2].

High speed, low power wireless data link has been investigated by previous published work [3], however there are still a lot of problems in power delivery: One of which is that how to reduce the ripple of the recovered dc source on the receiver chip, since only ac power can be transferred wirelessly and on-chip decoupling capacitor is not large enough.

We solve the problem by multi-phase approach. A number of power transmission channels work simultaneously with an appropriate phase shift so that their output ripple current cancels out to suppress the voltage ripple.

2. Test chip design

Fig.2 shows the circuit diagram of proposed system. It includes four power delivery channels and a control circuit. Each channel contains an H-bridge transmitter and an on-chip planar inductor for magnetic field generation on Tx chip, an on-chip planar inductor and a rectifier for DC power recovery on Rx chip. All the channels output are connected to an off-chip load and a filter capacitor in parallel. Clocks of the channels have a phase shift as 0, $\pi/2$, π , $3\pi/2$, so that the output current of each channel. All the channel acts as a current source to the load, and their current sums up on the load. The control circuit is used to switch on and off the channels, so that we can check the effects of each channel and combination of several channels.

Fig.3 illustrates the circuit of the power transmission channel. H-bridge transmitter generates ac current on the transmitter inductor, and then the inductor yields a changing magnetic field. In order to generate stronger field for power transmission, transmitter needs high current driven ability, thus a distinct shoot-through current will pass through M1 M2 (Fig.2) each switching transition. For preventing the shoot current, a switching control circuit is added to the hbridge transmitter as Fig.3. It makes sure M1 and M2 will not turn on simultaneously.

The inductor on the receiver senses the change of the magnetic field, produces ac current on the receiver. On-chip rectifier converts the ac current to on-chip dc source. To raise the power conversion efficiency we added a bias equals threshold voltage between gate and

source of the diode-connection MOSFET in the half wave rectifier [4]. The on-state voltage drop is lowered by V_{th} , so that conversion loss is decreased.

3. Simulation and measurement results

The system shown in Fig.2 was implemented in TSMC CMOS 0.18 μ m process. Fig.4 shows the microphotograph. The size of the on-chip inductors come in 600 μ m*600 μ m.

When test the chips, Transmitter chip and receiver chip are mounted on two PCB boards, and then face to face equipped on the micro-operator as shown in Fig.5. An infrared camera is used to makes sure the accuracy of the arrangement.

Fig.6 shows the relationship between received average current and frequency when load equals 200ohms. As the frequency increases from DC to 80MHz, the impedance of inductor (ωL) increases, so that more power is transferred rather than just turned to be heat on the resistance; as the frequency increases further, the leakage current on the capacitor becomes major factor, so that lower received power.

80 MHz is chosen as system clock, since maximum power delivery is get at that frequency. Output current of each channel is tested as in Fig.7. Due to the half wave rectifier, current only flows half of the Switch period.

It can be seen in Fig.8 with the multiphase scheme, we accomplished reducing ripple from 200mv at 1 channel to 15 mV at 4 channels.

4. Conclusion

By using multi-phase scheme we achieved 12mW power delivery in 0.18 μ m CMOS Process by 4 channels of 600 μ m*600 μ m coupled inductors and successfully reduced the ripple to 15mv with 100pF decoupling capacitor.

Acknowledgement

This work is supported by VDEC. The authors are grateful to M. Tago, M. Mizuno and Y. Nakagawa with NEC Corporation for their assistance in measurements.

References

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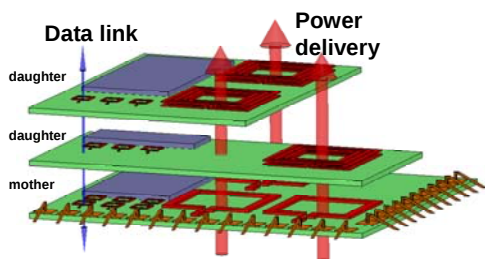


Fig.1 Conception of wireless SiP system.

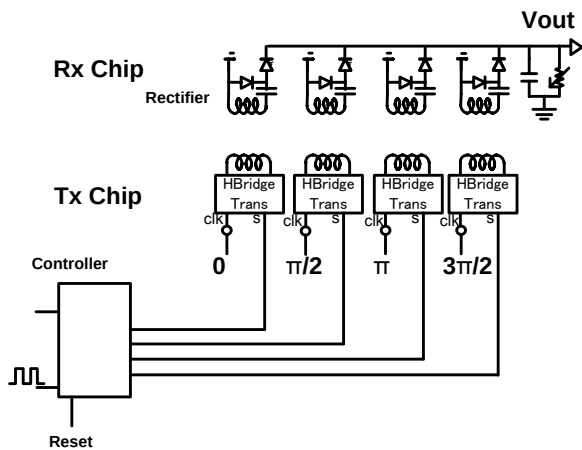


Fig.2 Circuits diagram of the system.

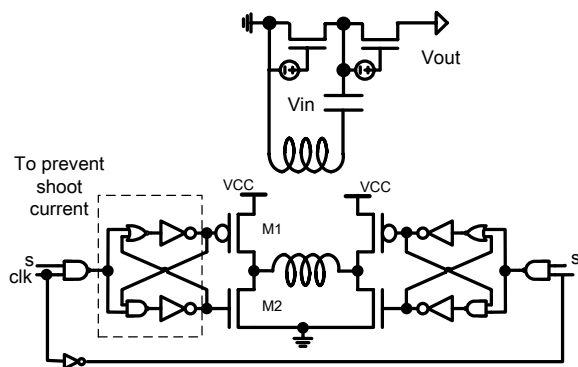


Fig.3 Circuits of the power delivery channel.

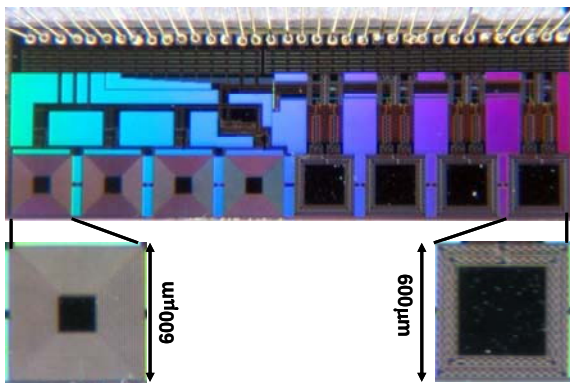


Fig.4 Microphotograph of the test chip.

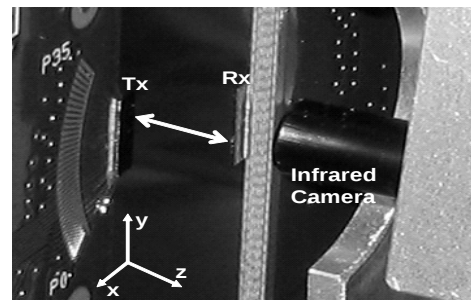


Fig.5 Measurement setup.

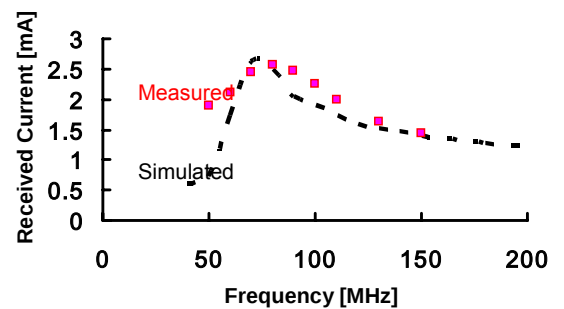


Fig.6 Received average current dependence on frequency.

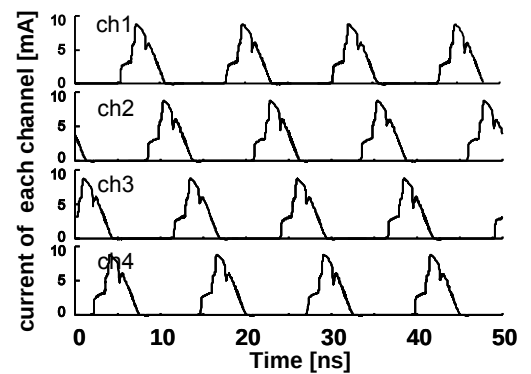


Fig.7 Output current of each channel.

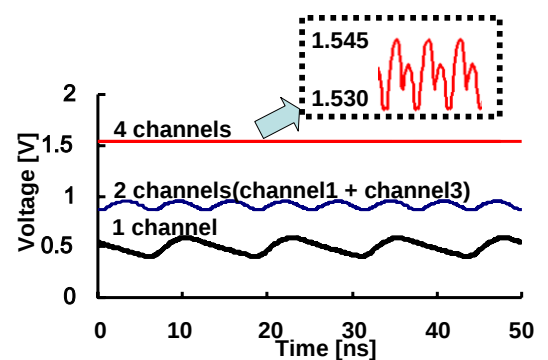


Fig.8 Output voltage dependence on the number of channels. (Rload =200ohms, C=100p)