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Tungsten Through-Si Via (TSV) Technology for Three-Dimensional LSIs

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1. Introduction

In recent years, three-dimensional (3D) integration technology has attracted much attention since it offers the possibility to solve interconnection problems. The 3D LSI has great advantages such as short wire length, high packaging density, high-speed operation, low power consumption, and high feasibility for parallel processing. We have previously fabricated 3D LSIs based on wafer-to-wafer, chip-to-chip, and chip-to-wafer bonding technologies [1-5]. One of the most important processes for 3D LSI is through-Si buried interconnection (via) formation. Buried interconnection (via) electrically connects between frontside and backside of Si substrate. The formation process of buried interconnection consists of deep-Si-trench etching, dielectric layer formation along the Si trench sidewall, and trench filling with conductive materials. In addition, deep Si etching through thick passivation layer deposited on LSI chips and low-temperature processes below 400 °C are strongly required for buried interconnection formation to avoid the heat damage to MOSFET.

In this paper, we describe Si etching, SiO_2 deposition and W filling processes for buried interconnection formation.

2. Fabrication process of 3D LSI

Figure 1 conceptually shows cross-sectional structure of 3D LSI fabricated using wafer-to-wafer 3D integration technology. In this figure, three LSI layers are vertically stacked and respective layers are electrically connected by a number of vertical interconnections composed of buried interconnections and metal microbumps. The wafer stacking sequence for wafer-to-wafer 3D integration technology is shown in Fig. 2. At first, an LSI wafer glued on supporting material is thinned from the back surface to expose the bottom of the buried interconnection, and metal microbumps are formed on the bottom of the buried interconnections. Then, the LSI wafer is aligned to another LSI wafer. After that, both wafers are bonded by metal microbumps. Epoxy adhesive is injected to the resulting gap between wafers to provide a strong bondability. By repeating this sequence, we can fabricate multiply stacked 3D LSI. Finally, the supporting material is removed.

3. Buried interconnection formation

The process flow of buried interconnection formation is shown in Fig. 3. After resist patterning, passivation layer and Si substrate are etched with a resist mask. The trench without any side etching at the interface between Si and SiO_2 layers or bowing is needed for the following deposition processes. After trench etching and resist removing, passivation layer is formed on the trench sidewall to insulate buried interconnection from Si substrate. Finally, a wiring material of W is conformally filled into the trench. High step coverage deposition of the dielectric and wiring materials are required for these processes. Moreover, as shown Fig. 3, buried interconnections are formed after MOSFET formation and multi-level metallization process, and thus, high temperature process can not be applied in the buried interconnection formation process. Deep-Si trench etching through passivation layers are formed by anisotropic dry etching. One of the major problems in deep-Si trench formation is the side etching. To solve this problem, a protection film is deposited on the sidewall of the trenches to reduce the amount of side etching [5]. Low temperature processes below 400 °C strongly requires the SiO_2 layer formation and metal filling. Many techniques are widely used for SiO_2 film formation at low temperature process, such as plasma enhanced chemical vapor deposition (PECVD) and atmospheric pressure chemical vapor deposition (APCVD). However, these techniques provide low step coverage to form SiO_2 layer into deep trenches for buried interconnections. To satisfy both high step coverage and low process temperature, TEOS/O_3 SACVD method is employed for our 3D integration technology. We have previously formed buried interconncetions filled with phosphorus-doped polycrystalline silicon (poly-Si) as conductive materials. However, resistance of poly-Si is not sufficiently low to apply to the wiring material in 3D LSI with high data rate. Moreover, high process temperature is needed to completely fill poly-Si into deep trenches. To solve this problem, time-modulated W CVD method was applied for complete filling [6]. The outline of time-modulated W CVD method is shown Fig. 4. In this method, WF_6 and SiH_4 gas are alternately provided and evacuating steps are inserted between the two gas providing steps. High step coverage can be realized using this method since surplus WF_6, SiH_4 and by-product are evacuated in the evacuating step and WF_6 and SiH_4 are provided to bottom of trench in the gas providing step.

4. Experimental results and discussion

Figure 5 shows an SEM cross-sectional view of the trenches with the protection sidewall film formed into the passivation layer of SiO_2. As shown in this figure, a protection film was little formed on the bottom of the

trenches. The protection films were formed on the sidewall surface of the SiO_2 trenches with a thickness of around 700 nm. The relationship between the trench width and the amount of side etching that is generated in the following Si etching is shown in Fig. 6. As is clear in this figure, the amount of side etching significantly increases with the decrease of trench width since the deposition rate of protection sidewall films decreases in the case of narrow trenches. Figure 7 shows an SEM cross-sectional view of the trench formed through the passivation layer of SiO_2. No side etching was formed when the trench width was more than 3um. This result leads to the complete filling of the deep trenches with conductive materials. The relationships between top trench area and step coverage of SiO_2 formed by $TEOS/O_3$ SACVD method are shown in Fig. 8. The step coverage is determined as a ratio of the bottom SiO_2 thickness to the top SiO_2 thickness of the trench. As shown in Fig. 8, although the step coverage decreased by scaling down the area, more than 60% of step coverage was obtained at trench with $10um^2$ of top area. Figure 9 shows an SEM micrograph of SiO_2 film deposited in the deep Si trench with $20um^2$ of top area at 350 °C of substrate temperature. As seen in the figure, step coverage of more than 70% was obtained in this SiO_2 film. The relationship between deposition temperature and step coverage of W formed by time-modulated W CVD method is shown in Fig. 10. The step coverage increases with a decrease in deposition temperature. Figure 11 shows an SEM cross-sectional view of trench filled with W using time-modulated W CVD method at 300°C. As is clear in this figure, more than 100% of step coverage was acquired using time-modulated W CVD method.

5. Conclusion

Buried interconnection formation processes including deep-Si-trench etching through passivation layer, SiO_2 deposition using $TEOS/O_3$ SACVD and time-modulated W CVD method for W filling were investigated. We successfully formed deep trenches through passivation layer, oxide layer with high step coverage, and conformal W layer under low temperature conditions.

Acknowledgments

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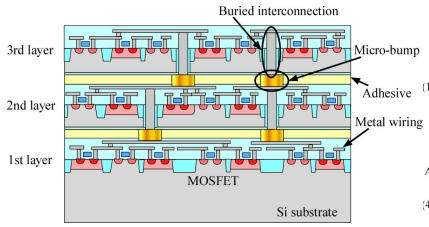


Fig. 1. Cross-sectional structure of 3D LSI.

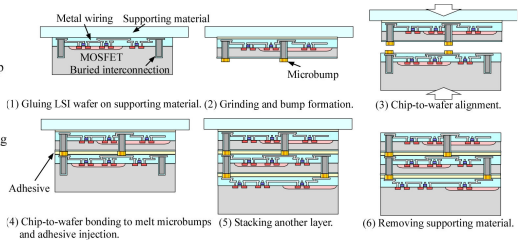


Fig. 2. Fabrication sequence of 3D LSI.

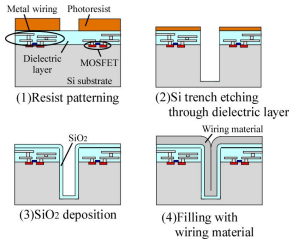


Fig. 3. Process flow of buried interconnection formation.

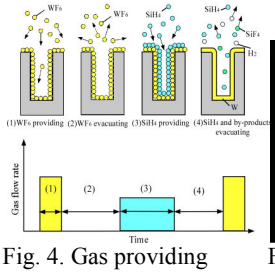


Fig. 4. Gas providing sequence of time-modulated W CVD method.

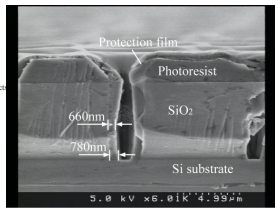


Fig. 5. SEM cross-sectional view of protection film.

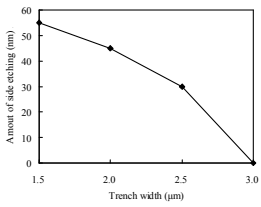
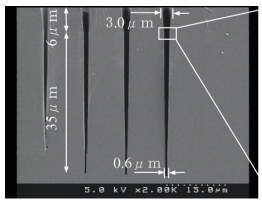


Fig. 6. Relationship between the trench width and the amount of side etching.



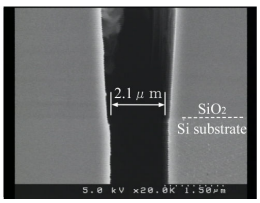


Fig. 7. SEM cross-sectional view of deep-Si trench through thick passivation layer.

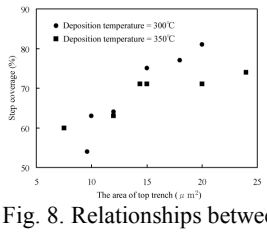


Fig. 8. Relationships between top area of the trench and step coverage of SiO_2 formed by $TEOS/O_3$ SACVD method.

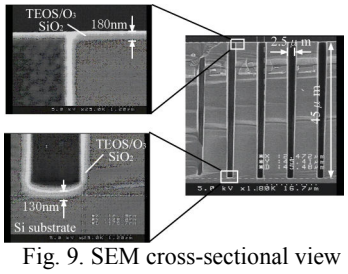


Fig. 9. SEM cross-sectional view of SiO_2 film formed by $TEOS/O_3$ SACVD method in the deep Si trench.

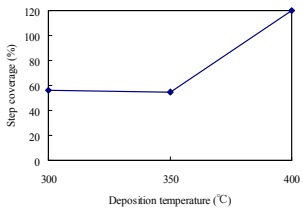


Fig. 10. Relationship between the deposition temperature and step coverage of W deposited by time-modulated W CVD method.

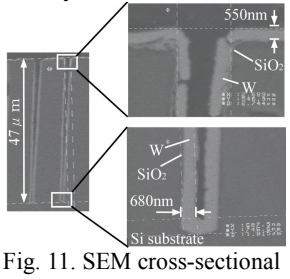


Fig. 11. SEM cross-sectional view of trench formed W using time-modulated W CVD method.