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Through-Only De-embedding for On-Chip Symmetric Devices

Yosuke Goto and Minoru Fujishima

School of Frontier Sciences, The University of Tokyo
5-1-5-703 Kashiwanoha, Kashiwa 277-8561, Japan
Phone: +81-4-7136-3846 E-mail: {yosuke,fuji}@axcel.k.u-tokyo.ac.jp

1. Introduction

Wireless communication using high-frequency carriers is required as increasing communication speed. In high-frequency integrated circuits, losses in wiring determine circuit performance. However, since performance of on-chip passive devices is often difficult to estimate only utilizing electro-magnetic simulations, the devices are characterized by measuring test devices before designing circuits. In the test devices, parasitic impedances of pads and lead wires have to be removed for extraction of nature characteristics of the device. This operation is called de-embedding. The most popular de-embedding is open-short de-embedding [1]. In the open-short de-embedding, parasitic elements in the device are assumed as serial and parallel lumped ones which are removed by measuring open and short dummy patterns. In this method, however, the assumption of lumped parasitic elements results in large error as increasing frequency. In order to realize high-accuracy de-embedding even in high frequency region, several methods were proposed [2-4]. Improvements of their de-embedding precision are achieved using complex model with many parasitic elements, which are characterized by many dummy patterns. Increase of dummy test patterns, however, will increase measurement errors and occupy large area. Here, for transmission lines, another de-embedding method was proposed to extract the characteristics from difference between two transmission-line test devices with different lengths, based on the distributed constants [5]. Applying this de-embedding to general symmetry devices, we propose new through-only de-embedding in this study. In the following sections, after describing a procedure of the through-only de-embedding, de-embedding accuracies are discussed. Finally, measurement results applying the through-only de-embedding are shown.

2. Procedure of Through-Only De-embedding

In the through-only de-embedding, device characteristics are calculated utilizing symmetric property of devices. It is noted that, in practice, most of on-chip passive devices have symmetric structures. As shown in Fig. 1, this method requires a main pattern including device under test (DUT) and a dummy pattern with the through structure whose length is equal to the lead wires of the main pattern. In this de-embedding, ABCD matrixes and admittance matrixes are used. The procedure has three steps. Assumed that F_{DUT} and F_{TH} are the ABCD matrixes of a main pattern including the DUT and a through dummy pattern, calculate F_{mid} as

$$F_{mid} = F_{DUT} \cdot F_{TH}^{-1}. \quad (1)$$

Secondly, F_{mid} is converted into an admittance matrix Y_{mid}. Here, $\mathrm{swap}(Y_{mid})$ is defined as the admittance matrix when ports 1 and 2 of Y_{mid} are swapped. Thirdly, the admittance matrix of the DUT Y_{DUT} is calculated by averaging Y_{mid} and $\mathrm{swap}(Y_{mid})$ as

$$Y_{DUT} = (Y_{mid} + \mathrm{swap}(Y_{mid}))/2. \quad (2)$$

The through-only de-embedding procedure is summarized in Fig. 2.

3. Estimation of De-embedding Errors

De-embedding errors are estimated by simulating the equivalent circuit model of an on-chip inductor with pads as shown in Fig. 3, where L_s is inductance, R_s is series parasitic resistance, C_{sub} is capacitance between the inductor and substrate, and R_{sub} is substrate resistance. Transmission lines, whose inductance is 21pH and resistance is less than 10mΩ, are used for modeling pads and lead wires. Device characteristics are extracted using the through-only and the open-short de-embeddings, the results of which are compared with the given inductor parameters. In this simulation, de-embedding errors are calculated as a function of L_s. Here, C_{sub} and R_s are adjusted proportionally to L_s, while R_{sub} maintains constant as 15Ω. Figure 4 shows a simulation example of inductances and quality factors using extracted and given parameters when L_s is 0.1nH. As shown in Fig. 4, the simulation results using the parameters extracted by the open-short de-embedding show discrepancy with those using the given parameters, while the results using the through-only de-embedding show no discrepancy. De-embedding errors of inductances and quality factors are summarized in Figs. 5 and 6, respectively, where the through-only de-embedding shows smaller error than the open-short de-embedding by more than order of magnitude. It is shown that distributed elements in lead-wires are effectively removed using the through-only de-embedding.

In this study, on-chip inductors, the micro photograph of which is shown in Fig. 7, were measured with a vector network analyzer. The measurement data are de-embedded using the through-only de-embedding and the open-short de-embedding. An example of the de-embedding result is shown in Fig. 8, where both inductances and quality factors using open-short de-embedding are larger than those using the through-only de-embedding. The errors of the open-short de-embedding become large as decreasing inductance.

4. Conclusions

The through-only de-embedding was proposed, which uses only a through dummy pattern. Since pads and lead wires can be modeled as distributed elements, the through-only de-embedding is suitable for the evaluation of passive devices in high-frequency region. The simulation results show that the through-only de-embedding has more than ten-times accuracy compared with the conventional open-short de-embedding. Using the through-only de-embedding, reduction of dummy patterns will not only suppress measurement errors but also save chip area, which is effective to reduce test cost.

References

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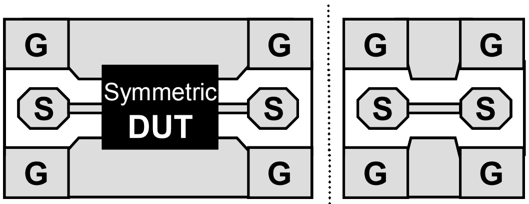

Fig. 1 Structures of the devices of (a) including symmetric DUT and (b) through dummy pattern.

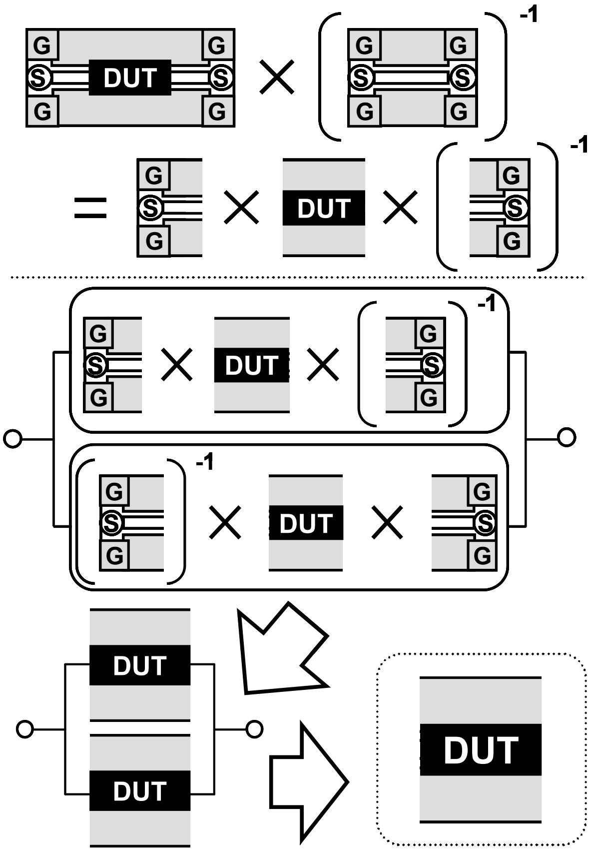

Fig. 2 Summary of through-only de-embedding.

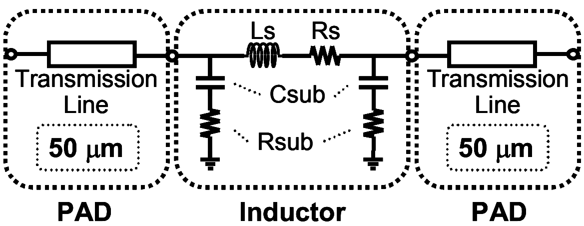

Fig. 3 Inductor test device model for the estimation of de-embedding errors.

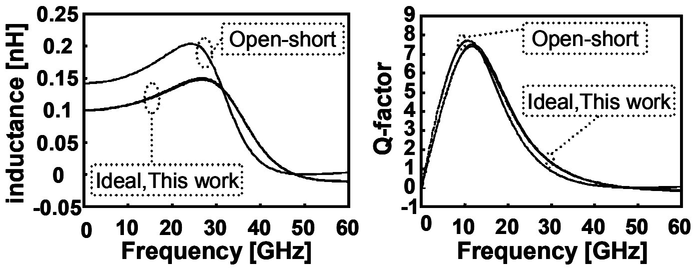

Fig. 4 The result of proposed method and open-short method when Ls = 0.1nH.

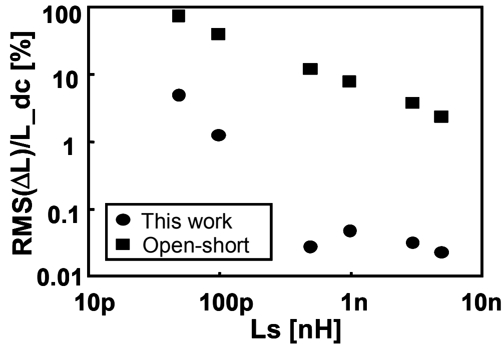

Fig. 5 RMS errors in inductances applying through-only and open-short de-embeddings.

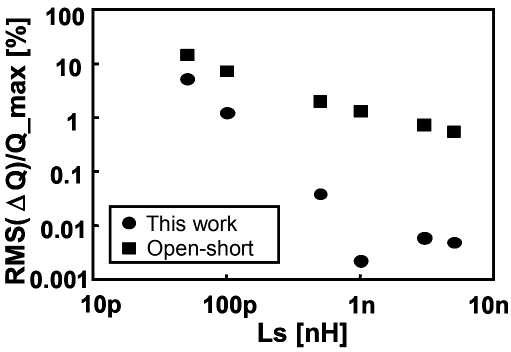

Fig. 6 RMS errors in quality factors applying through-only and open-short de-embeddings.

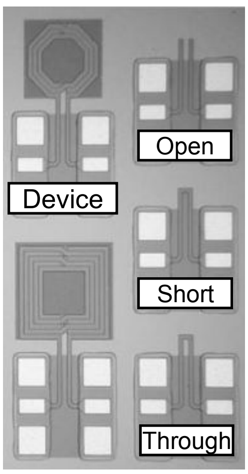

Fig. 7 Chip photo including measured TEG.

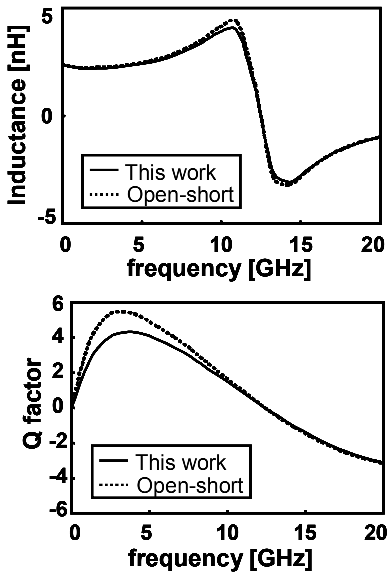

Fig. 8 Measured results of device applying two de-embedding